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Improving the performance parameters of Complementary Metal Oxide Semiconductor operational amplifier

A Thesis

Submitted to the College of Engineering / University of Babylon in Partial Fulfillment of the Requirements for the Degree of Master of Science in Engineering / Electrical Engineering / Electronic

By

Firas Sami Abdul-Kadhim Jabbar

Supervised by

prof. Dr. Hassan Jassim Motlak

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بسم الله الرحمن الرحيم

اللَّهُ نُور السَّمَاوَاتِ وَالأَرْضِ مَثَلُ نُورِهِ كَمِشْكَاة فِيهَا))
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صدق الله العلي العظيم

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ABSTRACT

There is a growing need for a high-performance CMOS OP_AMP is increasing needed for use in electronic and communications applications as well as in the biomedical field. For this purpose, OP-AMP must operate at wide bandwidth and high voltage gain with low power consumption to design a high-performance OP-AMP must select a technology to harmonize the process parameters of MOS FET transistors with the transistors. In this thesis, the main objective behind this proposed design is to reduce the low offset voltage to minimum value, so that its effect is reduced by a two-stage CMOS operational amplifier. Mostly operational amplifiers mainly consist of two inputs and one output. Practically no voltage appears on the output and the offset voltage is close to zero if there is no difference between the two input signals, at 180 nm TSMC technology. CMOS-OP-AMP is designed in three different approaches: Two-Stage, Folded Cascode, and third approach Telescopic OP-AMP. Simulation results are obtained using P SPICE (version 17.4.)2019 program. The results showed that the designed techniques are highly efficient in terms of a comparison of the three designs proved that the best design in terms of low power consumption, gain-bandwidth product (GBP) is the Telescopic CMOS OP-AMP. In terms of slow rate and settling time the two-stage CMOS OP-AMP is the best, as for the rate of improvement of the offset voltage, as the telescopic rate of improvement reaches 94 % and the two-stage reaches 70 %.

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ABBREVIATIONS

1	ADC	Analog To Digital Converter
2	BJT	Bipolar Junction Transistor
3	CMOS	Complementary Metal-Oxide Semiconductor
4	CMRR	Common Mode Rejection Ratio
5	IC	Integrated Circuit
6	MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
7	OP-AMP	Operational Amplifier
8	PSO	Particle Swarm Optimization
9	PSRR	Power Supply Rejection Ratio
10	TSMC	Taiwan Semiconductor Manufacturing Company
11	PM	Phase Margin
12	dB	Decibel
13	SR	Slew Rate
14	ICMR	Input Common Mode Range
15	UGB	Unity Gain Bandwidth

LIST OF SYMBOLS

Symbol	Description	Unit
Av	Voltage gain	-
Cc	Compensation capacitor	F
CL	Load capacitor	F
Cdb	Drain substrate parasitic capacitance	F
Cgb	Gate substrate parasitic capacitance	F
Cgd	Gate drain overlap parasitic capacitance	F
Cgs	Gate source overlap parasitic capacitance	F
Csb	Source substrate parasitic capacitance	F
Cgdo	Gate drain overlap parasitic capacitance per unit gate width	F/m
Cgso	Gate source overlap parasitic capacitance per unit area	F/m^2
COX	Gate oxide capacitance per unit area	F/m^2
GB	Gain bandwidth	Hz
GM	Gain margin	dB
g_m	MOS transistor V_{GS} to I_D transconductance	1/Ω
gmb	MOS transistor V_{SB} to I_D transconductance	1/Ω
gds	Output conductance of MOSFET transistor	1/Ω
ID	MOS transistor dc drain current	A
Kn	NMOS transistor transconductance parameter	A/V2
Kp	PMOS transistor transconductance parameter	A/V2
L	Channel length between drain and source	m
Pdis	Dissipation power	W
PB	Bulk junction potential	V

PM	Phase margin	degree
rds	Output resistance of MOSFET transistor	Ω
SR	Slew rate	V/s
Ts	Settling time	s
TOX	Silicon dioxide thickness of the MOS transistor	m
VT	Threshold voltage	V
VTo	Threshold voltage of V_T when V_{SB} = 0	V
VGS	Gate source dc voltage	V
VDS	Drain source dc voltage	V
V_{GD}	Gate drain dc voltage	V
VSB	Source substrate dc voltage	V
VDD	Positive supply voltage	V
VSS	Negative supply voltage	V
W	Gate width	m
XOV	Overlapping between the gate and source (or and drain)	m
XJ	Junction depth	m
ε_o	permittivity of the free space	F/m
ε_{sio_2}	silicon dioxide relative permittivity	F/m
µn	Electron mobility	m^2/(V.s)
µp	Holes mobility	m^2/(V.s)
γ	Bulk threshold parameter	V-1/2
λ	Channel length modulation parameter	1/V

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CHAPTER ONE

Introduction

1.1 Introduction:

The trend on the silicon chip has been for several main and basic reasons at the same time, including small size, used in all electronic devices, not consumed quickly, life is long, and it does not consume high energy [1], used in most electronic and industrial devices and is the basis for the manufacture of most devices, as well as in analogue devices. Used in most fields because its size is very small, and the power supply needs very small to operate [2][3].It is possible to obtain a little power consumption by making the size very small, but this affects the general performance, so the supplied voltage should be few, and the circuit parts be compressed to obtain a high speed, as well as to reduce the power dissipation [4].

Operation amplifier is one of the most used electronic parts in most fields and in the IC industry and in most electronic devices for several reasons that are important at the same time, including its small size, does not require high currents and does not consume high power [5], and can find the operational amplifier in one or two stages, depending on the use you need, and it is also used as a comparator, or for other parameters such as addition or subtraction and many more [6]. Commonly used in basic and main circuits such as integrator, voltage comparator and transformer analog digital converter, digital analog converter (ADC, DAC) and many more [7].

When we want a high profit in the circuit use one stage or two-stages or more, one of more and the most famous is the circuit that consists of two stages, which consist of two inputs and one output that used in our research, when a mismatch occurs between the components of the CMOS, a so-called offset voltage appears, and this affects the resolution and speed of the device [8], and there are two types of offset voltages, namely input offset voltage and output offset voltage [9].

1.2 Why use CMOS Op-Amp design:

Amplifiers are one of the main things in analog systems, as they can perform filtering operations, converting from analog to digital and vice versa, buffers and so on [10]. Therefore, the need to design the operation amplifier, the output signal is always much greater than the input signal, and from other applications in which it is used. In control, automation, as well as electronic circuits, CMOS has many advantages one of the most important advantages MOSFET is small in size, more than 10 times faster than transistors, and the effect of heat in it is less and the opening current is smaller compared to the transistor [11]

1.3 Problem statement affecting of CMOS:

There are many parameters that affect the work of the MOSFET, including common-mode rejection ratio (CMRR), noise, offset voltage, temperature, slow rate, and many other parameters that mainly affect the work of CMOS [12], in this thesis one of these parameters is taken and studied and its effect is found. And make designs to reduce its impact on the circuit.

1.4 Disadvantage of offset voltage:

When a mismatch occurs between the components of the CMOS, a so-called offset voltage appears, and this affects the resolution and speed of the device [13]. There are two types of offset voltages, namely input offset voltage and output offset voltage , the first is preferred in applications with high resolution and the second in applications that have a high speed. There are several ways to eliminate the offset voltage, auto-zeroing method, chopping, trimming and correlated of the double sampling etc [14].

1.5 Literature Survey:

Daniel DZAHINI and Hamid Ghazlane (2002), the design was designed using 800 nm technology, with an input voltage from 2 µV to 100 nV and the source voltage is 2.5 V and the value of the bandwidth was 2 MHz, and the method used is continuous time of auto-zero [15]

Masaya Miyahara and Akira Matsuzawa (2009), the design was done using a new dynamic, and the proposed design achieves a low offset voltage. The 90 nm technology was used and it achieved good results in the design, as the value of the offset voltage was 3.8 µV with a voltage source of 1.2 V at 500 MHz [16]

Heung Jun Jeon and Yong-Bin Kim (2010), the proposed design of a comparator that is used to reduce the offset voltage, and two inverters were added and were placed between the input and the output stage, the design was achieved by 90 nm with a 1V voltage source, the displacement voltage improved by 19 percent and less sensitivity by 62 percent.[17]

Heung Jun Jeon et al (2011), a dynamic comparator was analyzed and according to this analysis, the offset voltage value was reduced from I2.5mV to 6.5mV with an increase in the energy dissipated value of 9% .Using capacitive offset calibration, using a digitally the controlled the capacitive offset for the calibration technique through technology, the offset was reduced to 1.10 mV after it was 6.5 mV [18]

Chi-Hang Chan et al (2011) Low-noise designs were presented and the offset value was low, and the comparator ADC was used to reduce noise and offset, as the offset was improved from 11.6mV to 533µV and was used 90 nm technology at a frequency 1.5GHz and the power supply 1.2 V [19].

Heung Jun Jeon and Yong-Bin Kim (2012), the comparator of the dynamic latched with the offset voltage, the comparator need one clock signal for operation and the result the gain is 22dB, power supply 1V and using 90 nm technology offset voltage is reduced 24.6% less from (6.03 -1.1) mV [20].

Samaneh Babayan-Mashhadi and Reza Lotfi (2012), A new method was used to cancel the offset, and this method is to adjust the body voltage by using a circuit analog with control feedback with low-power, the 0.18 nm technology is used with 1.8 V power supply the offset is decreasing (36.2 to 7.1) mV [21].

Mohsen Hassan pourghadi et al (2013), the comparator was designed with positive feedback, the mismatch that occurs between the circuits determines the ratio between speed, offset and energy consumption, the design was done using 180 nm and 90 nm technology, and the resulting offset value was one-third of the value and the energy consumption value was 44 percent power consumption is 51µW and the offset voltage is 15.1mV [22]

Meysam Mohammadi Khanghah and Khosrov Dabbagh Sadeghipour, (2014) A new high-speed design comparator has been proposed, using A new boost method, simulated by Montecarlo method, using 180 nm technology, power dissipates 34 µW, voltage source is 0.5 and the offset voltage value is 0.288 mV [23].

V. Raghuveer et al (2017), a mechanism for reducing offset voltage is discussed, using a continuous of the zero-automatic amplifier, and an offset voltage of 2µV was obtained and the gain value was 131 dB, the bandwidth was 1.5 MHz and the power supply was 1.8 V [24].

L.Kouhalvandi (2017), the comparator was designed that enjoys high speed and accuracy, and the design was made using 180 nm technology and a voltage source of 1.8 V, the monticarlo method and angle and the use of 100 samples and 9 angles were used, and this design is suitable for use in conversion from analog to digital in electronic applications [25].

Avaneesh K. Dubey, and R.K. Nagaria (2018), designed CMOS with low power high-speed the used bulkdriven method., this method for low power result in reduced transconductance, the used 45 nm CMOS technology and with 0.8 V power supply the offset voltage is 1.05 mV [26].

P.P. Gandhi and N. M. Devashrayee (2018), The comparator was designed to obtain a better improvement in the value of the offset voltage, and the results were verified by Monte Carlo, and the results showed that the proposed system is 45% faster and the rate of improvement of the offset voltage is 91%, and using 180 nm technology and a voltage source of ± 0.9 [27].

G¨unhan D¨undar et al (2019), designed the circuit for determine direct current (DC) offset cancellation (OC) on the amplifier subject to aging and an identifier of his performance percentage the designed in low power with 40 nm Technology and power supply is 1.1 V the gain 22.2 dB and offset voltage 14.42 mV [28].

Robert Chen-Hao Chang et al (2019), designed a low offset voltage by used a constant on–time buck converter with 3.3V power supply and using 0.18um CMOS technology, the reduced the offset voltage to 8mv with high efficiency 93.4 % [29].

Kasi Bandl et al (2020) The are design circuits using successive approximation register (SAR) – ADC (analog to digital converter) the was used 180 nm CMOS technology with power supply 1.8V and the offset voltage is 6 mV [30].

Emad Alnasser (2020) was proposed circuit for reduce the offset voltage of the output he used conventional charge of the amplifier to reduce the offset the gain of the circuit is 20.5 dB and the offset voltage of output 5 mV [31].

1.6 Objective of the thesis:

The aim of this paper is to reduce the offset voltage, which mainly affects speed and resolution. Designs were made using the Orcad P-SPICE program (17.4) and using the 180 nm technology.

1.7 The thesis structure:

The thesis consists of five chapters and can classified as follows:

- In the first chapter, the literature survey, the introduction and background of the thesis, and its objectives are presented
- In the second chapter, the theoretical part is discussed, presenting the requirements for the manufacture of the CMOS, as well as the knowledge of offset voltage, its impact, types, and ways to reduce it.
- In the third chapter, three types of circuits are designed and simulated
- In the fourth chapter, the proposed design is made and the offset voltage is reduced
- In chapter five, recommendations for future work and conclusion are made.

CHAPTER TWO

Theoretical of CMOS Operational Amplifier Design

2.1 Introduction:

The OP-AMP is a basis using the analogue circuit, and it's more popular with it. Designs Op-Amp different in complexity levels this is according to the use of each design to achieve filtering and high-speed amplification. One of the most used devices today and used in the fields of scientific It is considered one of the most basic and main ingredients in use in both digital and analogue circuits and evenly. Operational amplifiers are widely used in most electrical appliances like integrators, voltage comparators, filters, converters also (ADC, DAC) [32].

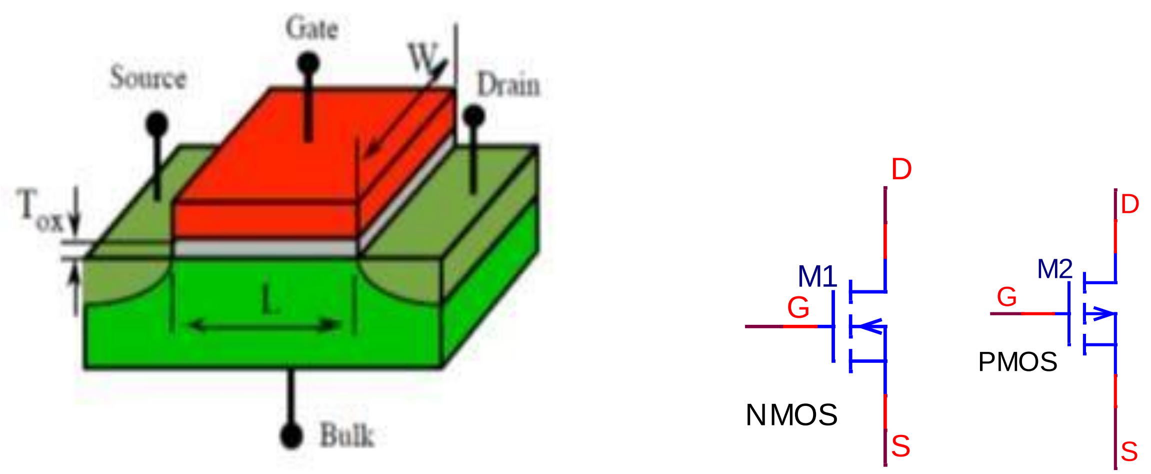
2.2 The fabrication of MOSFET (MOS) components:

MOS technology is a technique by which the components of the MOS can be implemented and is considered the basis for designing most circuits, including the operation circuit, as well as the manufacture of IC.

2.2.1 MOS transistor:

The transistor is a three-terminal device, and in MOSFET type the fundamental principle of its operation depends on the fact that the current flowing in one terminal is controlled by the voltage across the other two terminals. So to obtain a controlled source which is very important in amplifier design, the CMOS transistor become essential element. Also can change the current value in the third terminal by varying the amount of the control signal so can use it as switch. MOSFET are better than BJT in more than one property such as small size and lowest power consumption. The new smart techniques make the designers able to construct the digital and analogue devices to implement advanced digital and or analogue circuits like storage units, microprocessors, amplifiers [33].

Figure (2.1a) shows the general structure of the a MOSFET transistor the MOSFET consists of drain (D), source (S), gate (G), and the bulk terminal (B). All these four terminals are active regions. The upper part is the rectangular gate that is insulated with a very small layer of oxide insulator of as much TOX the bottom material is the silicon substrate the two other important dimensions are width and length [34].



(a) (b)

Figure (2.1) (a) The MOSFET structure (b) The MOSFET symbols.

MOSFET NMOS and PMOS are the two types that make up the MOSFET. The source and the drain are of the same type in both types, but the difference is of the type N-type in NMOS and the type P-type in PMOS semiconductors and also in the polarity of the carrier in the NMOS electrons are charged carriers while in the PMOS holes are charged carriers and forms of the two types in the Figure (2.1b) [34]

The start of construction of the transistor with the doped substrate, the substrates of MOS which doped with n-doped is PMOS, while p-doped is NMOS the gate end is electrically isolated from the gate end is electrically isolated from. The crystalline semiconductor structures under which the thin Transistor Oxide (Tox) is shown in Figure (2.2), the amorphous silicon that forms amorphous forms the gate oxide, SiO_2 amorphous. The typical range is 15Å to the 100 Å of the thickness (Tox) of the gate oxide, there is an insulator of SiO_2 between the drain and the source allowing the charge to pass through them. The quantity of charge passing between the source and the drain resulting from electric field that is generated by the gate voltage as a result of the SiO_2 dielectric, the gate oxide thin allows the electric field of the gate to better faster transistors and also control the device state.[35]

The source is n-doping, as well drain is n-doping too in NMOS while in PMOS p-doping the substrate (bulk) is opposite to the source and drain in doped, Figure (2.2) showing the structures of PMOS and NMOS.

Figure (2.2) Schematic of the transistor (a) NMOS doping (b) PMOS doping transistor.

Channel length is the distance between the drain and source and denoted by the symbol (L), the width is denoted by (W), as shown in Figure (2.1a) [35].

2.2.1.1 The characteristics MOSFET:

To calculate properties of the MOSFET draw drain source voltage (V_{DS}) versus drain current (I_D) for a number of overvoltage values, express the limit between saturation (active region) and a linear (Ohmic region) by (V_{GS} – VT); that appear in the curved drawing the NMOS transistors are measurements for number curves in Figure (2.3) [35].

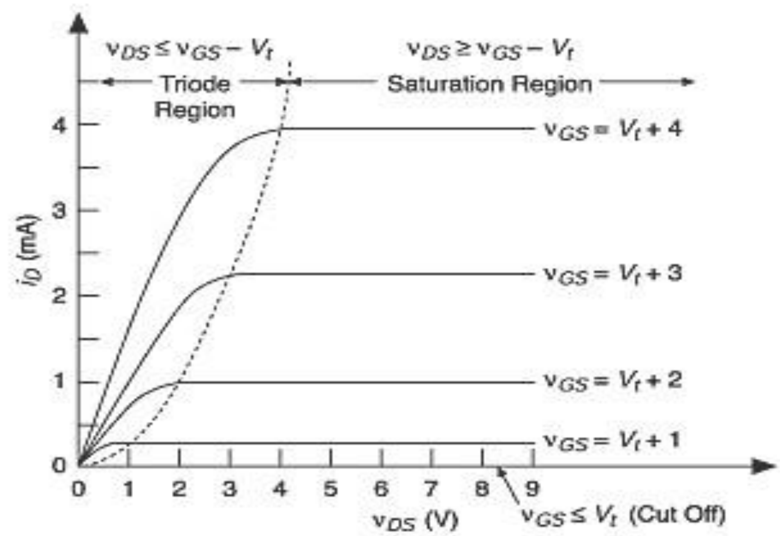


Figure (2.3) Output NMOS characteristics [35].

Where the transistor is ON, two connection modes were marked saturated and unsaturated flat part is the curve that shows saturation region when the $V_{GS} < V_{DS} + V_{Th}$ NMOS become in the region of the saturation , and (I_D) in this case it does not depend on V_{DS} While $V_{GS} > V_{DS} + V_{Th}$ NMOS in the non-saturation, when ($V_{GS} < V_{Th}$), for any value of V_{DS} the I_D is zero, the transistor will off .The current I_D is increase linearly from the initial value before bending this called liner region or ohmic region [35]

From V_{DS} - I_D characteristics notes that there are three operation regions

- Saturation region at $V_{GS} < V_{DS} + V_{Th}$.
- Linear region (ohmic region) at $V_{GS} > V_{DS} + V_{Th}$.
- Cut off at $V_{GS} < V_T$

2.2.1.2 Equivalent small-signal circuit of a MOSFET:

In linear applications, voltage and current vary such (operational amplifiers) we cannot be overlooked capacitive effects the device can be used with small signals and all non-linear relationships. Linear approximation can be done MOSFET analysis of the saturation region will be demonstrated because MOSFET is often in this aspect or case it is biased in its behavior to linear applications and its action is in saturation the equivalent circuit shown in Figure (2.4) [36].

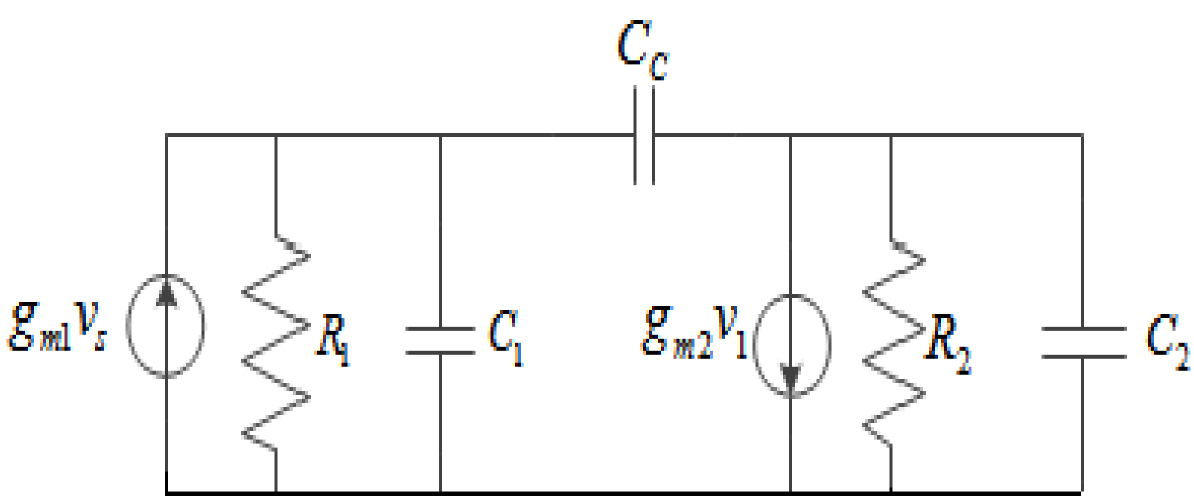


Figure (2.4) Equivalent circuit of small signal of MOSFET Op-Amp

In the following equations, the properties of MOSFET are shown in the saturation state and in the enhancement mode [37].

$$I_D = \frac{K_n}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \qquad (2.1)$$

$$K_n = \mu_n C_{OX} \qquad (2.2)$$

$$g_m = \sqrt{2K_n\left(\frac{W}{L}\right)I_D} \qquad (2.3)$$

$$g_m = 2\sqrt{\frac{K_n}{2}\left(\frac{W}{L}\right)I_D} \qquad (2.3a)$$

$$g_m = K_n\left(\frac{W}{L}\right)(V_{GS} - V_T) \qquad (2.3b)$$

$$g_m = \frac{2I_D}{V_{GS} - V_T} \qquad (2.3c)$$

$$g_{mb} = \lambda g_m \qquad (2.4)$$

$$V_T = V_{To} + \gamma\left(\sqrt{-V_{SB} + 2\emptyset} - \sqrt{2\emptyset}\right) \qquad (2.5)$$

$$C_{gs} = W C_{OX}\left(X_{OV} + \frac{2}{3}L\right) \qquad (2.6)$$

$$C_{gd} = W C_{OX} X_{OV} \qquad (2.7)$$

$$C_{gb} \approx zero \qquad (2.8)$$

$$g_{ds} = \lambda I_D \qquad (2.9)$$

where:

ID : DC drain current

VDS : DC drain to source voltage

VGS : DC gate to source voltage

where:

VSB : DC source to substrate voltage.

VT : Threshold voltage.

VTo : The value of VT when VSB = 0

COX : Gate oxide capacitance per unit area.

µn : Electron mobility(for NMOS transistor).

µp : Hole mobility(for PMOS transistor).

Kn : NMOS transistor transconductance parameter (KP for PMOS)

Since the amount of each of Cgb and Csb small usually neglected. They are frequently ignored in PMOS transistor characteristics equations should be reversed

2.3 Operational amplifier:

Operation amplifier is one of the most used electronic parts in most fields and in the IC industry and in most electronic devices for several reasons that are important at the same time, including its small size, does not require high currents and does not consume high power. It consists of three-terminal, there are two inputs inverting and the other is a non- inverting whose resistance is high and one output, the operation's amplifier performs several tasks, including subtraction, comparison and many others Figure (2.5) shown block diagram of the Op-Amp [38].

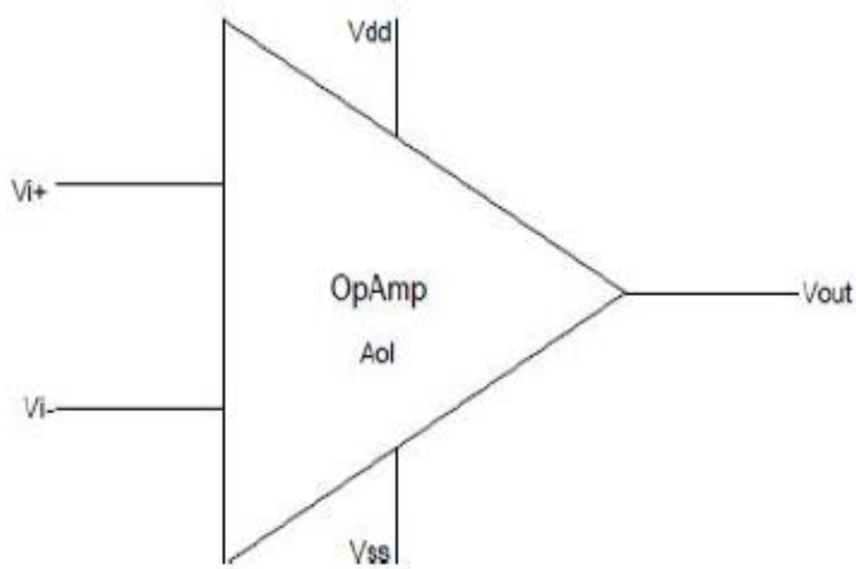


Figure (2.5) Op-Amp of block diagram

2.3.1 Two-stage Op-Amp:

Operation amplifier can find in one or two stages, depending on the use you need, and it is also used as a comparator, or for other parameters such as addition or subtraction and many more Figure (2.6) shown the general block diagram [39].

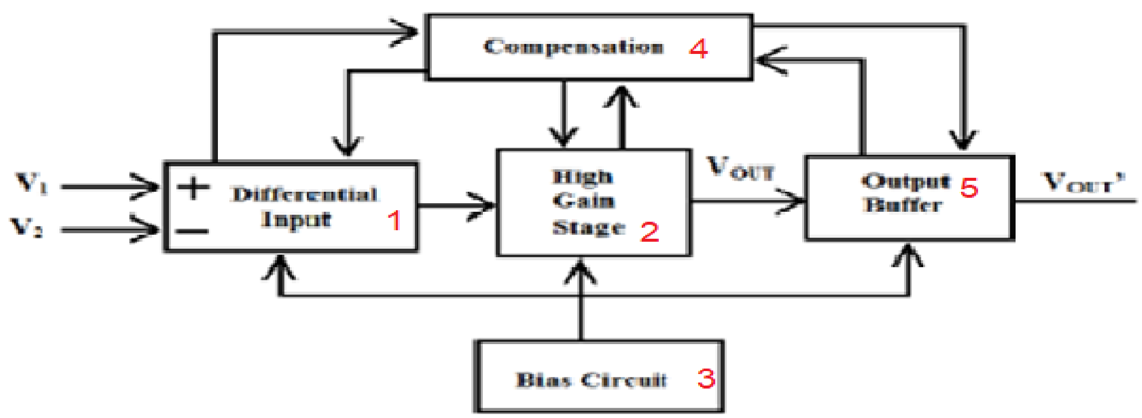


Figure (2.6) Block diagram of two-sage

The differential amplifier is the first blocks which consists of inverted voltage and non-inverted voltage. The second single-ended converter the signal generated in first blocks convert to single-ended. The provided gains in input stages mostly are not sufficient the solution to this problem is to add extra amplification .The third blocks bias circuit is provided to create an operating point in the saturation for each transistor. The fourth blocks compensation tie first stage with second stage it basically is capacitor. The fifth stage is output buffer stage that has larger output current and low output impedance used to drive the load or improve the slew rate in most cases, can dropped output stage because in most cases do not use low resistance in the output and in most applications, the Figure (2.6) shows the circuit of the two -stages Op-Amp [39, 40].

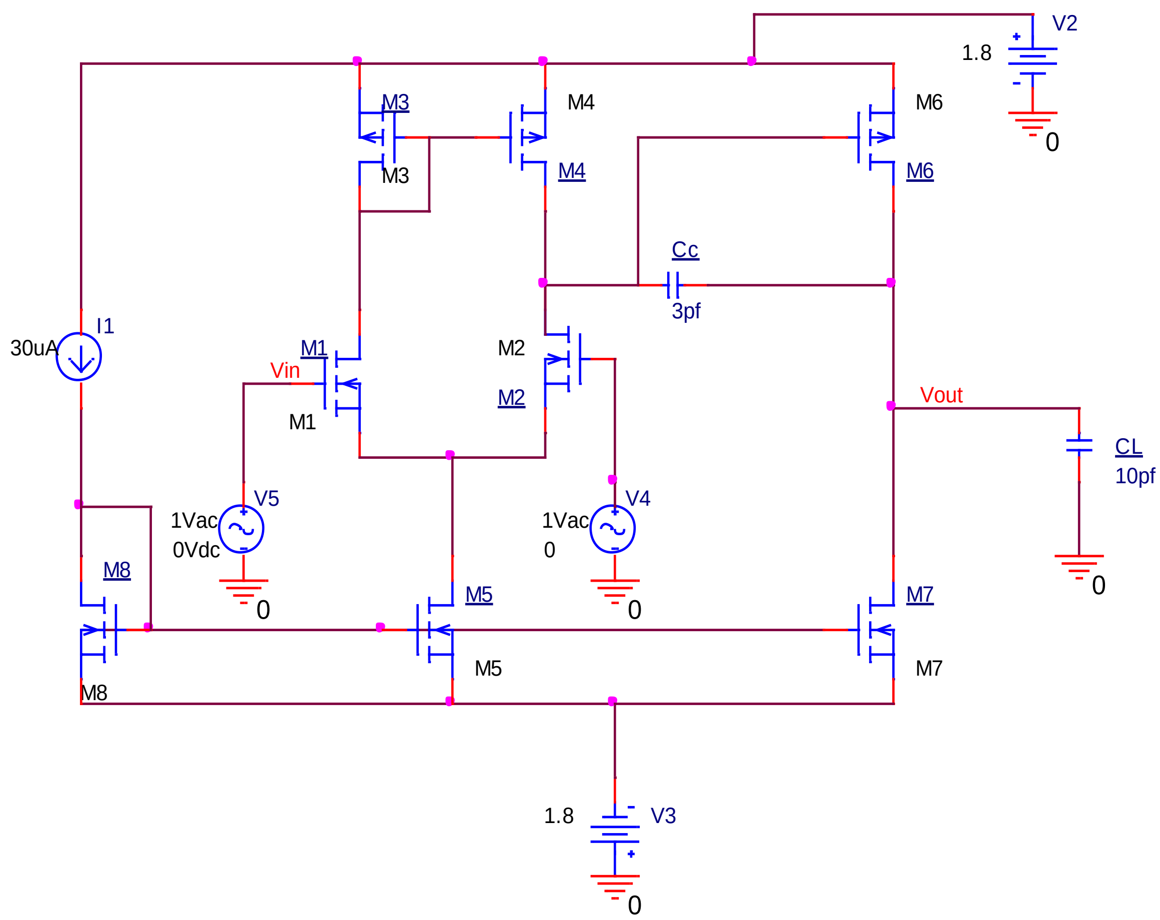


Figure (2.7) The circuit of the two-stage CMOS

2.3.2 A telescopic Op-Amp

A telescopic Op-Amp is one of the other types of operating amplifiers that is distinguished from the rest of the designs in terms of power consumption and other advantages is the frequency. One of the disadvantage is that it limited swing in the output Figure (2.8) telescopic circuit of the CMOS Op-Amp [41].

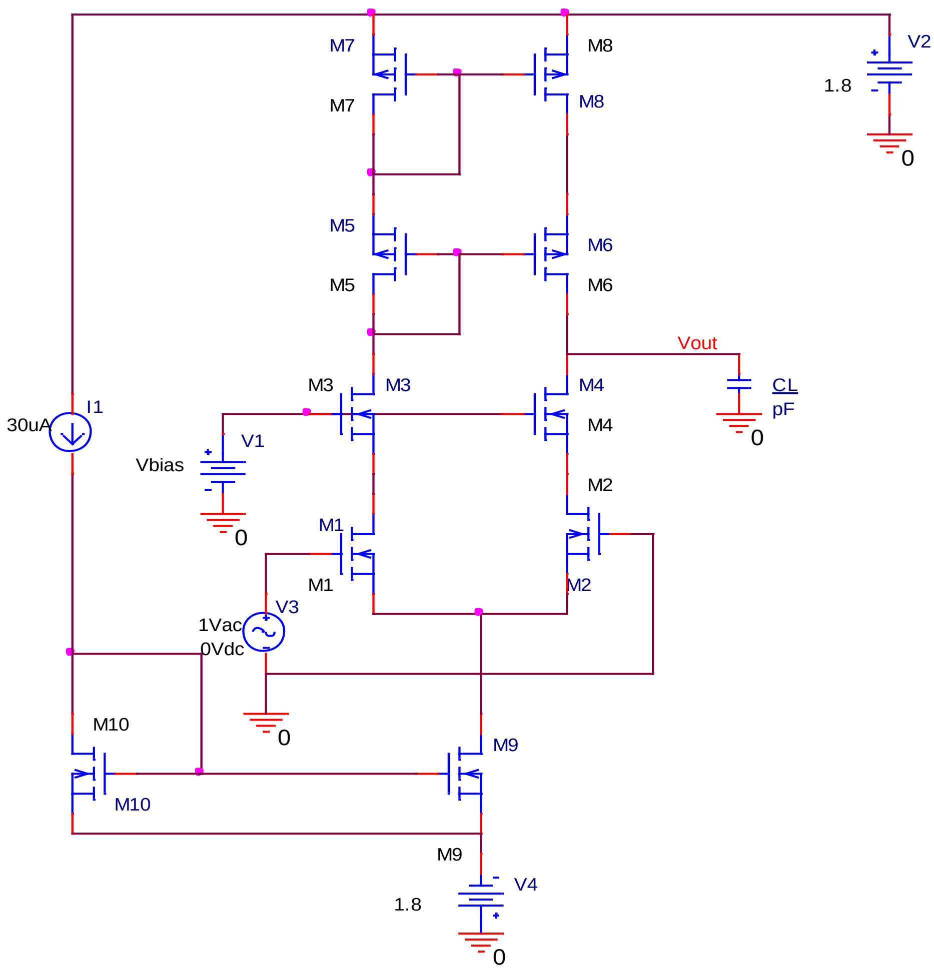


Figure (2.8) The telescopic circuit of the CMOS Op-Amp.

2.3.3 A Folded cascode amplifier self-biasing Op-Amp:

It is another type of amplifier that is unipolar which is very high in terms of swing in the output and larger than telescopic, as well as the gain is high. Then deal with the equations in the next chapter. Figure (2.9) represents the folded circuit [42,43].

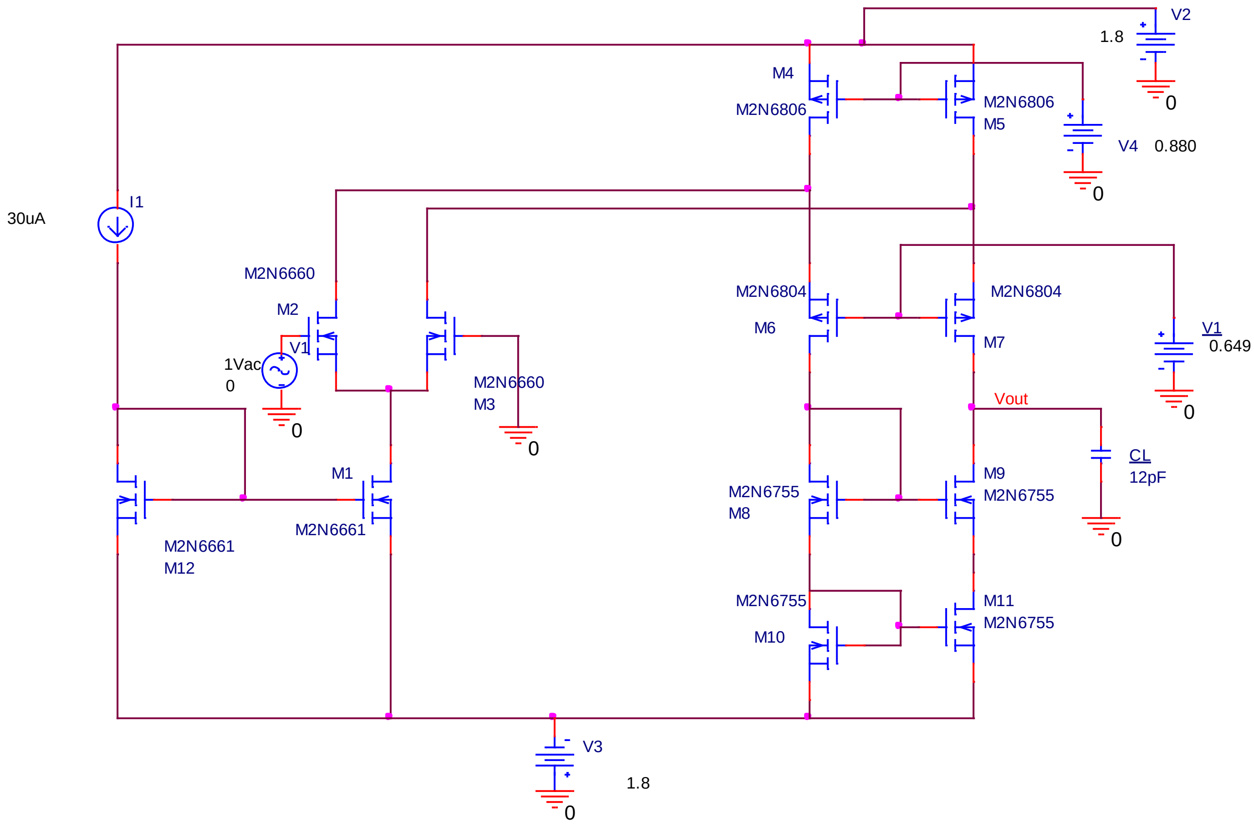


Figure (2.9) Folded cascode CMOS Op-Amp amplifier.

2.4 The general considerations of the operation amplifier:

2.4.1 The current sink and current source:

A current sink is an outlet or point of a circuit that accepts a negative current, for example the current that passes through the circuit ground. The current source is an outlet or a circuit point that provides a positive current for example of a DC power source. In the case of the source current the output is capable of providing current while in the basin current it is capable of receiving the current, and often the source current is negative at (V_{SS}) and positive at (V_{DD}) Figure (2.10) shows current source and current sink [44].

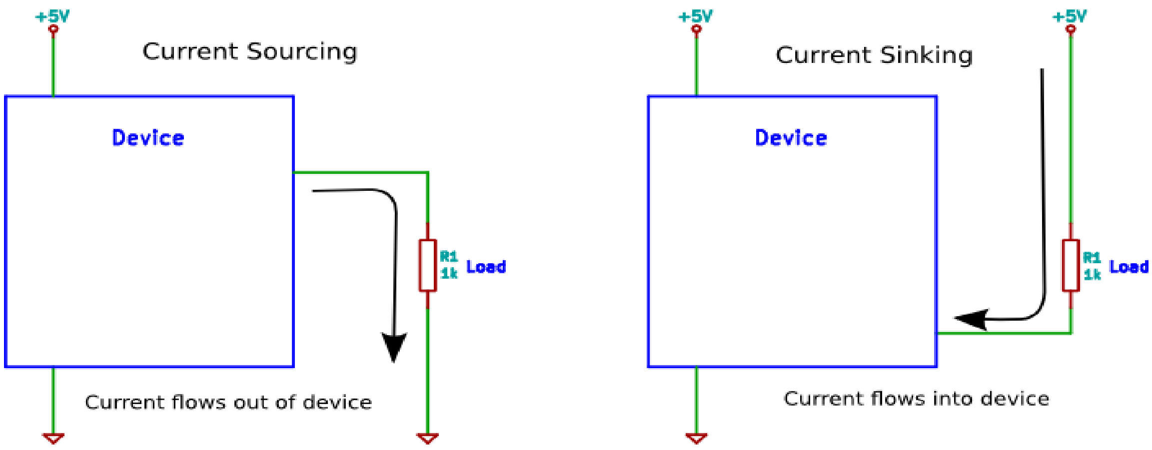


Figure (2.10) Current source and current sink

2.4.2 Current Mirror:

It was obtained from a single transistor current using a second the transistor in diode connection which generates the necessary voltage for source transistor gate at the output stage. The principle is gate -source capabilities of two type of MOS transistors are identical, the channel current must be taken into account Figure (2.11) explain the NMOS current mirror, current I_{in} is current source and I_o is the "mirrored" current [45].

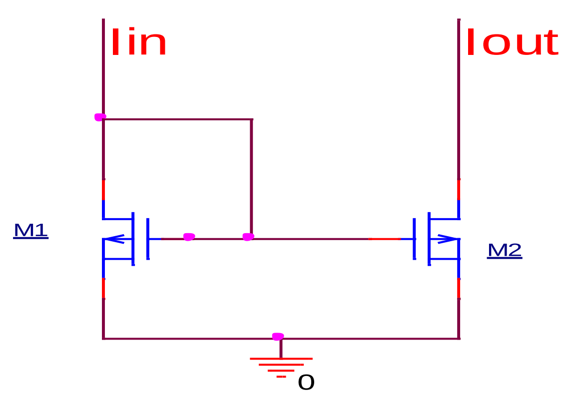


Figure (2.11) Simple current mirror.

M_2 in saturation region M_1 is in saturation region too since $V_{DS1}=V_{GS1}$ on the same integrated circuit be processed the current mirror components thus all parameters like V_T and k are identical ratio of I_o/I_{in} shown in equation.

$$I_o = \frac{W_2 L_2}{W_1 L_1} I_{in} \tag{2.10}$$

2.4.3 The Slew Rate and Settling Time:

Slew rate is the expression or product of the change in voltage or current with respect to time and its unit is volts / second, either in the case of current it is amperes / second or any other electrical quantity, but most often it is (V / µs) and as the following law

$$\mathrm{SR} = \max\left|\frac{dv_{\mathrm{out}}(t)}{dt}\right| \tag{2.11}$$

Settling time: One of the important parameters that is the time required for the system or circuit to be stable, or the time the circuit needs to reach the output or

0.5% of its final value [46].

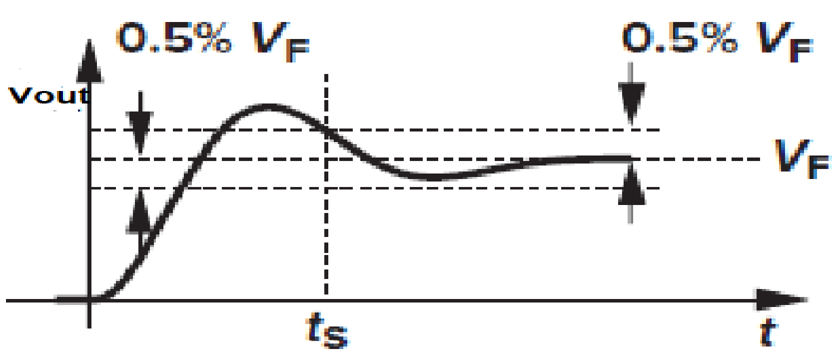


Figure (2.12) Settling time definition

2.4.4 DC biasing:

There are several types of circuits that are used to make bias, including connecting two types of transistors, one of which is type (PMOS) and the other is (NMOS) type. As shown in the Figure (2.13) below, the circuit connection process.

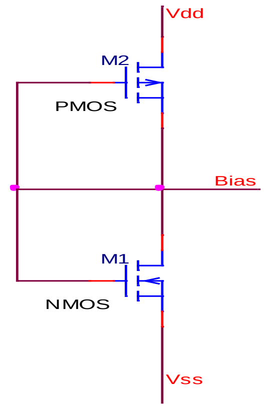


Figure (2.13) Bias of circuit of two-stage

As for the other type of circuit, which we use in our research, it is to replace the transistor of type PMOS and put a current source, and consists a current source and a transistor of type NMOS and as shown in the Figure (2.14) below the connection process of the circuit. [47].

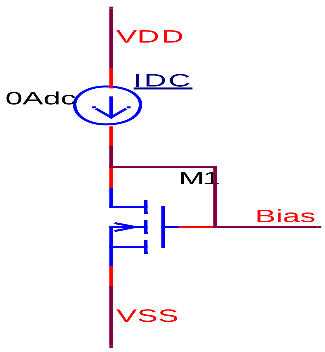


Figure (2.14) Bias of circuit of two-stage

2.4.5 Frequency compensation:

In general, in order to get a good response to the frequency, we need more than one stage, and with the increase in the number of stages the poles increase, and these poles help in reaching the phase angle to 180 degrees and to increase the stability of the phase margin as well as the closed loop the circuit must be modified and this process is called compensation [48].

The illustrated method that is explained is "Miller" compensation this is done by tied capacitor from the output to the input two-stage CMOS amplifier compensation and output small signal model the results of adding the (Cc) is the effective capacitance increased by gm2(R2)(Cc)

This change p1 and p2 to new of the location (p'1, p'2) significantly in this case it is far from a status resulting collector and close to the status of complex frequency from reducing of output resistance and negative reactions [49].

2.5 Mismatch:

In theory, we could get differential amplifiers that are identical in terms of characteristics, but in practice this is not possible because it is difficult to obtain the same properties in factory, the following Figure (2.15) shows the difference that occurs, and the difference that occurs between length and width [49].

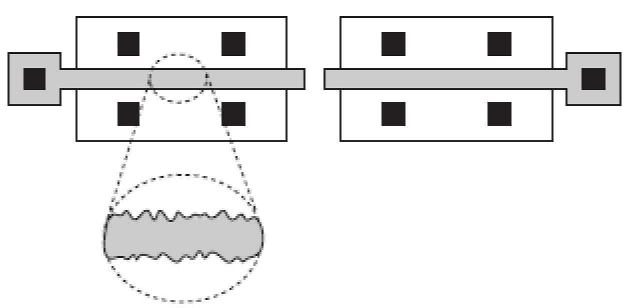


Figure (2.15) Mismatches between dimensions of the MOSFET

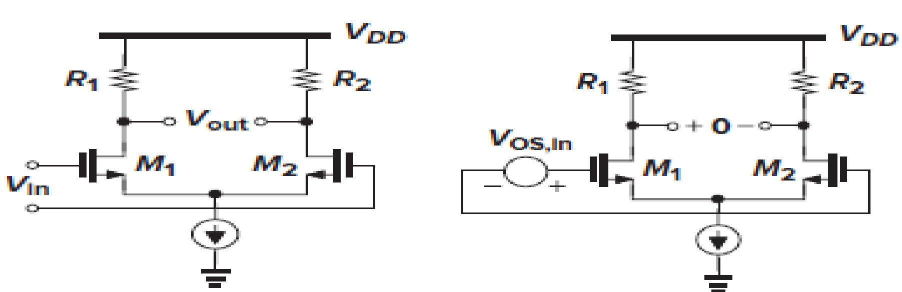
In the study of mismatch, you have to know two important things, the first is to know the reasons that lead to the mismatch, and the second is to know the problems that occur due to the mismatch between the components, In the first part it is difficult to achieve because it is manufactured. In the following equation (2.1), any difference in the components (μ, Cox ,W, L, and VT) leads to the mismatch that occurs between the discharge streams.

$$ID = (1/2)\mu Cox\ (W/L)(VGS - VT\ H)2 \quad (2.1)$$

A very important note is that the greater the area of the transistor, the more the mismatch disappears [49].

2.5.1 The Effect of Mismatch:

The mismatch affects the performance of the circuit, and the mismatch leads to the emergence of three phenomena, the first is DC displacement, the second is the regular distortion in the arrangement and the last is the rejection of the common situation, when the input source is equal to zero and output of the circuit equal to the zero, this case that the match is perfect, but in the case of mismatch and the output value is equal to zero , this case that there is an offset, where the offset voltage is defined as the input level that makes the output equal to zero ,the Figure(2.16) shown the differential pair[49].



(A) (B)

Figure (2.16) Differential pair with (A)offset at o/p (B) offset at i/p

Assume that have a small input effort and according to the shape we have identical copies of the signal as well as of the offset, and one of the most important effects of offset is to restrict the accuracy with which the signal can be measured Figure (2.17) shows the effect of offset in an amplifier [49].

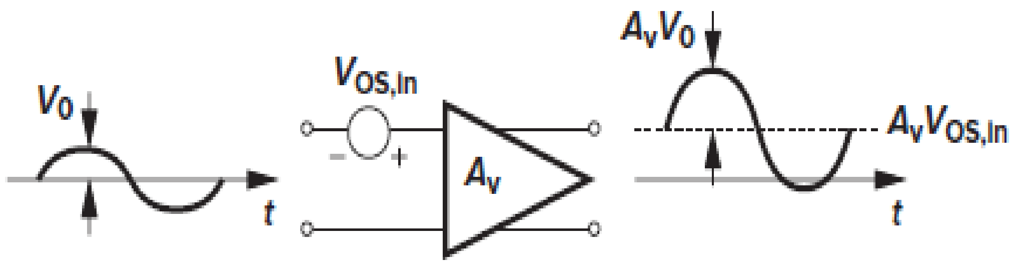


Figure (2.17) Effect of offset in an amplifier.

To order to calculate the input offset voltage of a differential pair, the input transistor and load resistors are mismatched, it is based on the following equations [49].

$$V_{OS,in} = V_{GS1} - V_{GS2} \tag{2.12}$$

$$V_{os.in} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH1} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} - V_{TH2} \tag{2.13}$$

$$= \sqrt{\frac{2}{\mu_n C_{ox}}}\left[\sqrt{\frac{I_D}{\frac{W}{L}}} - \sqrt{\frac{I_D + \Delta I_D}{\frac{W}{L} + \Delta\left(\frac{W}{L}\right)}}\right] - \Delta V_{TH}$$

$$= \sqrt{\frac{2}{\mu_n C_{ox}}}\sqrt{\frac{I_D}{W/L}}\left[1 - \sqrt{\frac{1+\frac{\Delta I_D}{I_D}}{1+\Delta\left(\frac{W}{L}\right)/\left(\frac{W}{L}\right)}}\right] - \Delta V_{TH}$$

Assuming that $\Delta I_D/I_D$ and $\Delta\left(\frac{W}{L}\right)/\left(\frac{W}{L}\right) \ll 1$ and noting that for $\epsilon \ll 1$ we can write $\sqrt{1+\epsilon}\ \approx 1+\epsilon/2$ and $\left(\sqrt{1+\epsilon}\right)^{-1} \approx 1-\epsilon/2$, we reduce

$$V_{os.in} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}\left\{1-\left(1+\frac{\Delta I_D}{2I_D}\right)\left[1-\frac{\Delta(W/L)}{2(W/L)}\right]\right\} - \Delta V_{TH} \tag{2.14}$$

$$= \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}\left[\frac{-\Delta I_D}{2I_D}+\frac{\Delta(W/L)}{2(W/L)}\right] - \Delta V_{TH}$$

Where the product of two small quantities is neglected. Recall that $I_{D1}R_1 = I_{D2}R_2$,and hence $I_D R_D = (I_D+\Delta I_D)(R_D+\Delta R_D) \approx I_D R_D + R_D \Delta I_D + I_D \Delta R_D$. Consequently, $\Delta I_D/I_D \approx -\Delta R_D/R_D$, and

$$V_{os.in} = \frac{V_{GS}-V_{TH}}{2}\left[\frac{\Delta R_D}{2R_D}+\frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH} \tag{2.15}$$

2.6 Parameters affecting of CMOS:

There are many parameters that affect the operation of the MOSFET, which have an effect on its work, such as noise, temperature effect, offset voltage, (CMRR), (PSRR) and other parameter we are limited in this research to one type of these parameters, which is the offset voltage, which we know about its types and its effect on the circuit and ways to reduce it [44].

2.6.1 Offset voltage (Vo):

When a voltage source is placed on the inverting part or the non-inverting part, the output of the circuit is equal to zero, practically not possible because it is the mismatch between components that causes this to the unwanted voltage [49].

2.6.1.1 Offset voltage types:

There are two types of offset voltage, the first is the input offset voltage the second is the output offset voltage and already knew that offset is one of the harmful parameters in the circuit, it affects the resolution and the speed. In the applications that modify the resolution we use input offset voltage and in the applications that need to modify the speed used output offset voltage [26].

2.6.1.2 Methods for eliminating offset voltage:

As we already knew that offset voltage has a detrimental effect on the circuit, so we must look for ways to reduce or eliminate the offset voltage, there are many methods that are used to reduce the offset voltage such as [26].

- auto-zeroing method
- chopping
- trimming
- correlated of the double sampling

2.7 Stability of CMOS parameters:

The increase or decrease in the open loop gain process until the system becomes un stable in the closed loop condition and this is called phase margin, larger systems gain margins can withstand system parameters to make larger changes, note that the unit gain in volume equals zero gain in decibels, the difference between phase curve and -180 degrees is phase margin, phase margin equal to or greater than 45 the system will stable [49].

2.8 Method of the offset cancelation technique:

The Figure (4.1) shows the proposed design that consists of several parts to form the final design, which consists of (G mi), which is a differential pair also consists of a resistance (R1) which is the load and consists of (A2) which is a second amplifier, all these three elements that we mentioned represent two-stage. It also consists of the auxiliary amplifier(A aux) and the (Gm, aux) which act as a feedback to the circuit . Vos1 represents the voltage applied to the main amplifier circuit and the second voltage VOS2 is the primary voltage of the auxiliary circuit, and these two voltages are the inputs of the circuit, the action of the switches is open during an operation canceling. In the following equations that link the input and output voltages.

$$V_{out} = \pm V_{os1} G_{m1} - (V_{in}^{+} \pm V_{os2}) A_{aux} G_{m,aux}] R_1 A_2 \tag{2.16}$$

$$V_{out} = \frac{(V_{in}^{+} + V_{os2})A_{aux}G_{m,aux}R_1A_2 \pm V_{os1}G_{m1}R_1A_2}{A_{aux}G_{m,aux}R_1A_2 - 1} \quad (2.17)$$

$$V_{uot} \cong V_{in}^{+} + V_{os2} \pm \frac{V_{os1}G_{m1}}{A_{aux}G_{m,aux}} \quad (2.18)$$

The offset voltage from the equation is

$$V_{out} - V_{in}^{+} = V_{os2} \pm \frac{V_{os1}G_{m1}}{A_{aux}G_{m,aux}} \quad (2.19)$$

The capacitor (C) performs the process of storing the voltages of (A aux) and the switches in this state are closed and the voltage value is as follows.

$$V_{out,tot} = \frac{V_{out} - Vin_{in}^{+}}{G_{m1}R_1} \quad (2.20)$$

Substituting the previous Eq (4.4) into this Eq (4.5) yields

$$V_{out,tot} = \pm\frac{V_{os2}}{G_{m1}R_1} \pm \frac{V_{os1}}{G_{m1}R_1A_{aux}}\left[\frac{G_{m1}}{G_{m,aux}}\right] \quad (2.21)$$

If the A aux

$$A_{aux} = \frac{G_{m1}}{G_{m,aux}}$$

Then the output offset voltage equal to the equation

$$V_{os,tot} = \frac{V_{os1}}{G_{m1}R_1} + \frac{V_{os2}}{G_{m1}R_1} \quad (2.22)$$

$$V_{out,tot} = \frac{1}{G_{m1}R_1}(\pm V_{os2} \pm V_{os1}) \quad (2.23)$$

So that we get the lowest error, the values of (G m, aux) are much less than the value of (G mi) and the voltages are very small until a match occurs with the devices, depending on the two equations [50].

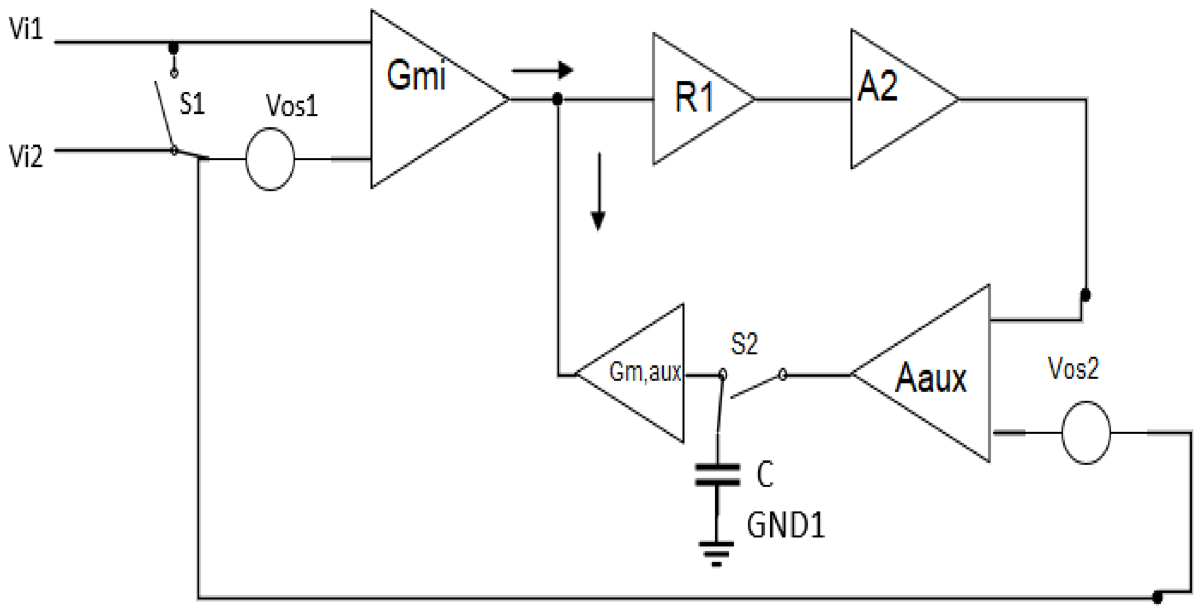


Figure (2.18) Architecture of the proposed circuit cancellation technique

CHAPTER THREE

The Design Of CMOS Operation Amplifier

3.1 Introduction:

As we mentioned earlier that an Op-Amp consists of one output and two inputs, and one of the inputs is inverted and the other is inverted, and here the two stages circuit will be designed using the P- SPICE program with 180 nm technology and extract all values such as gain, offset voltage and phase, etc. Design the proposed circuit, as well as with the same program and the same technology, and compare the resulting results before and after putting the proposed circuit, Figure (3.1) shows a diagram of the general shape of the design.

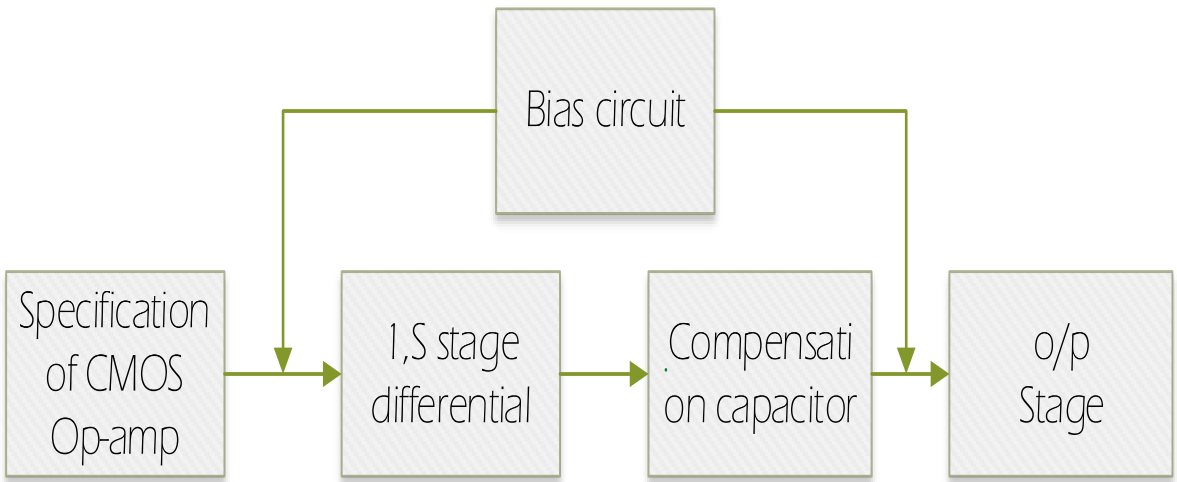


Figure (3.1) The general block of the design

In the first part, the specification of each MOSFET such as (Tox, K, V_{To} etc), in the second part the circuit is calculated for the first stage, which is the differential stage that has a high gain, and before all this there must be a bias for the circuit and this third part, which consists of a current source and a MOSFET of the type NMOS, and in the next part is the stage of the combination capacitor that is tie differential stage with the output of the circuit, the last part is the output through which the circuit simulation is performed.

3.2 Design of CMOS two-stage operation amplifier:

Two-stage circuit is designed, where the circuit consists of two sources, positive (V_{DD}) and the other is negative (V_{SS}), as well as containing an AC source and capacitive that connects between the first stage and the second stage called (Cc) and the another capacitive (CL) in the load of the output for the second stage, and the Figure (3.2) shows this circuit [1].

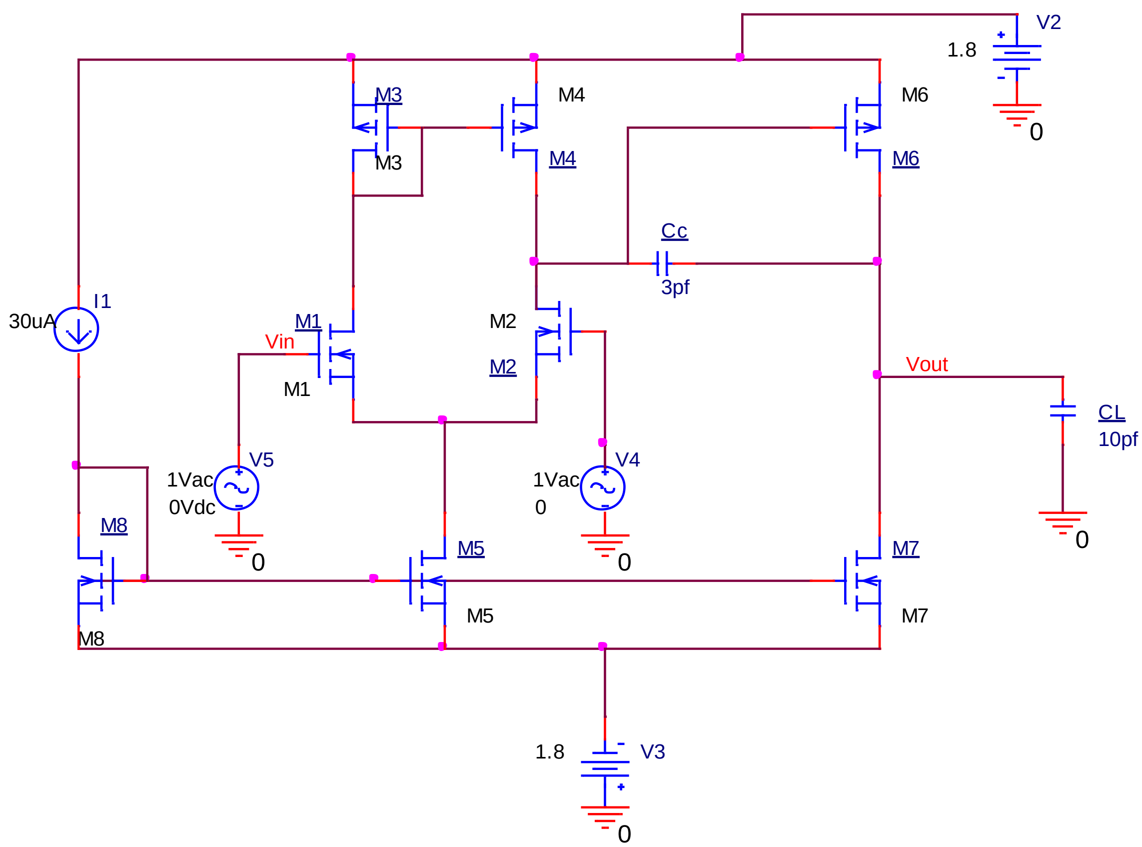


Figure (3.2): Schematic the design of the circuit CMOS two-stage

Where (M1-M7) are MOSFET, C2 is load capacitor, C1 is compensation capacitor, V2, V3 dc voltage, V4, V5 AC Voltage, I1 DC current.

In two stage design and other designs there are some fixed parameters in the design, the parameters for the design that works in 180 nm technology and these parameters are for both types (NMOS) and (PMOS) as shown in the Table (3.1) [51].

Table (3.1) The parameters of two-stages CMOS

parameter	NMOS	PMOS	Unit
Level	3	3	-
Tox	140	140	A
XJ	0.2	0.2	um
K	110	50	uA/V2
V_{To}	0.55	-0.8	V
λ	0.01	0.01	1/V
C_{gbo}	700E-12	700E-12	F/m
Cgso	220E-12	220E-12	F/m
C_{gdo}	220E-12	220E-12	F/m

3.2.1 Specifications of the two-stages CMOS operation amplifier:

The important part in the design process is the specifications that the circuit operates like gain band width, slew rate, power supply, phase margin and capacitor of the load as shown in the below Table (3.2).

Table (3.2) Fixed specification with circuit of the CMOS two-stages Op-Amp.

Parameter	value
Power supply	±1.8
Slew rate	10 V/μs
Channel length	180 nm
Load capacitance	10 pF
$\mu_n c_{ox}$	110 μA/V^2
$\mu_p c_{ox}$	50 μA/V^2
Gain Bandwidth	5 MHZ
Phase margin	60°

3.2.2 Design parameter of CMOS two-stage operation amplifier:

The circuit shown in Figure (3.3) was designed with a 180 nm technology and the circuit was designed by Orcad 17.4 software, and in order to design a circuit of two stage you must follow the following methods

- Selecting the basic structure of the Op-Amp

- Choosing of the dc currents and MOSFET sizes
- Choose the parameters and know their measurements

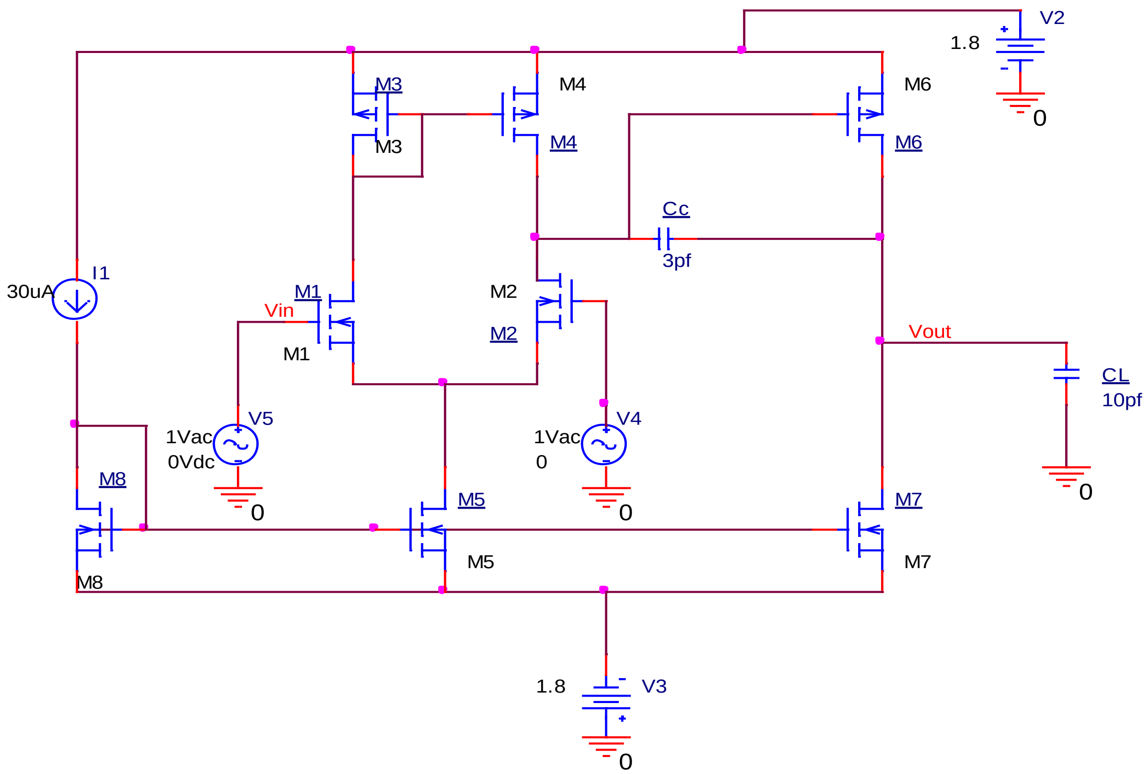


Figure (3.3) Represents the two-stage Op-Amp circuit.

First, the principal equation has to be extracted by Kirchhoff Current law (KCL)

$$\frac{v_o}{v_i} = \frac{A_{DC}(1-\frac{s}{z})}{1+s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)+s^2\left(\frac{1}{p_1 p_2}\right)} \tag{3.1}$$

By observing the previous equation, we can learn and extract most of the equations that we need by designing and the beginning of the rest of the other equations First stage gain.

Input pole, $P_1 = \frac{1}{g_{m2} r_{o2} r_{o1} c_c}$ (3.2)

Output pole, $p_2 = \frac{g_{m2}}{c_2}$ (3.3)

Zero $Z = \frac{g_{m2}}{C_c}$ (3.4)

Slew rate $SR = \frac{I_5}{C_c}$ (3.5)

Voltage gain $A_{DC} = g_{m1} g_{m2} r_{o1} r_{o2}$ (3.6)

Gain Band width, $GBW = \frac{g_{m1}}{c_c}$ (3.7)

Some specifications are fixed and must be placed before the design in the two-stage circuit, such as slew rate, gain bandwidth, and others as shown in Table (3.2).

Design calculate the ratio between width to length of the all CMOS MOSFET in the circuit, according to the Table (3.2) the values are placed and the values of the equations are extracted [1,3,8].

$$C_c = \frac{2.2}{10} C_L \quad (3.8)$$

$$I_5 = SR(C_C) \quad (3.9)$$

$$g_{m1} = GB(C_c) \quad (3.10)$$

$$S1,2 = (\frac{W}{L})1,2 = \frac{g^2 m_1}{(K^{-}1)(I_{5})} \quad (3.11)$$

$$S3,4 = (\frac{W}{L})3,4 = \frac{I_5}{(K^{-}{}_3)[V_{DD} - V_{in}(max) - |V_{To3}|(max) + V_{T1}(min)]^2} \quad (3.12)$$

$$V_{Dss} = V_{in}(min) - V_{ss} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(max) \quad (3.13)$$

$$S5 = (W/L)5 = \frac{2(I_{5})}{K^{-}{}_5 \ (V_{Dss})^2} \quad (3.14)$$

$$g_{m6} = 2.2(g_{m2})(C_L/C_c) \quad (3.15)$$

$$S_6 = \left(\frac{W}{L}\right)6 = S_4 \frac{g_{m6}}{g_{m4}} \quad (3.16)$$

$$\mathbf{I}_6 = \frac{g^2{}_{m6}}{2\,K^-{}_6 S_6} \quad (3.17)$$

$$S_7 = \left(\frac{W}{L}\right)7 = S_5 \frac{\mathbf{I}_6}{\mathbf{I}_5} \quad (3.18)$$

Where:

VTo	Threshold voltage
μn	Electron mobility
μp	Holes mobility
λ	Channel length modulation parameter
SR	Slew rate
Kn	NMOS transistor transconductance parameter
Kp	PMOS transistor transconductance parameter
L	Channel length between drain and source

3.3 Design of telescopic operation amplifier:

It is very similar to a single-phase as shown in Figure (3.4). The currents are entered into the common gate and by means of the differential input pair, the transistors in the form of layers until achieving the telescopic configuration.

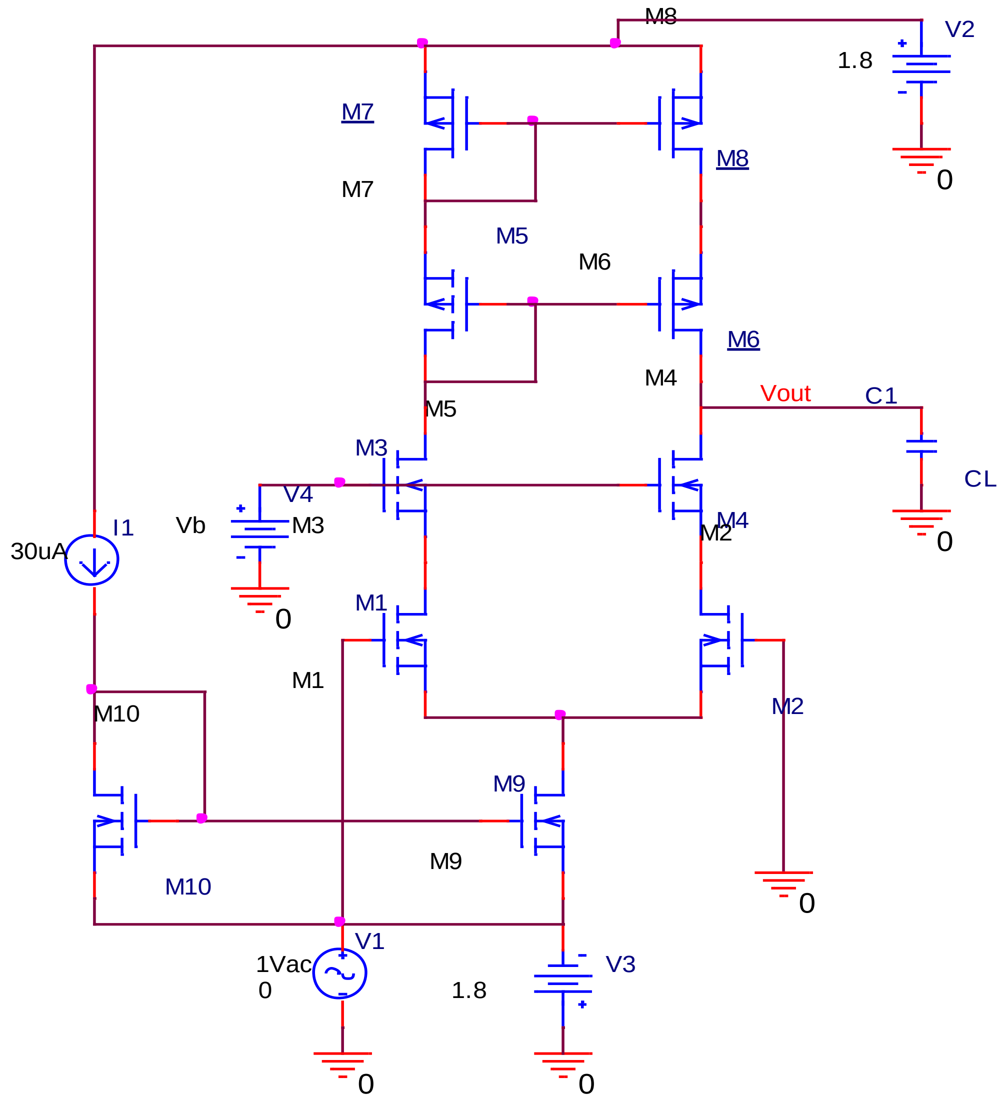


Figure (3.4) Schematic telescopic design of Op-Amp

The oscillation value of this type is very small, and this leads to a low dynamic range, and this type of the Op- Amp is considered one of the best types in the noise filtering process in which the noise is low, one of the most important defects of the telescope is its small swing in the output, which is less than folded Cascode [6].

All transistors in the proposed design are in saturation state until good CMRR is achieved for the circuit and the gain is good and high, etc.

3.3.1 The specifications of the telescope Op- Amp

The specifications that the circuit operates like gain band width, power supply, phase margin and Capacitor of the load as shown Table (3.3)

Table (3.3): The specification of telescopic Op-Amp.

No	**Specification**	**Values**
1	Gain	>45dB
2	Gain Bandwidth	5 MHz
3	(V_{DD}, V_{SS})	±1.8V
4	Phase Margin	≥60°
5	Load Capacitor	5pF
6	$\mu_n c_{ox}$	110 μA/V²
7	$\mu_p c_{ox}$	50 μA/V²

3.3.2 The equation of the telescopic:

Note the small signals whose frequency is reduced, and the gain is proportional to the resistance output, the design shall be according to the Table (3.7) and according to the following equations [3.19 to 3.25]

$$A_V = g_{m1} \frac{r_{ds8} g_{m6} r_{ds6} r_{ds2} g_{m4} r_{ds4}}{r_{ds8} g_{m6} r_{ds6} + r_{ds2} g_{m4} r_{ds4}} \qquad (3.19)$$

$$GB = \frac{g_{m1}}{C_L} \tag{3.20}$$

$$I_{D9} = 0.5K_n\left(\frac{W}{L}\right)[V_{GS} - V_{Tn}]^2 \tag{3.21}$$

$$I_{D1} = 0.5I_{D9} \tag{3.22}$$

Transistors (M5) through (M8) are the same so their values are equal

$$(W/L)_5 = (W/L)_6 = (W/L)_7 = (W/L)_8 \tag{3.23}$$

The values of [(M1) and (M2)], [(M3) and (M4)] are also equal

$$(W/L)_1 = (W/L)_2 \tag{3.24}$$

$$(W/L)_3 = (W/L)_4 \tag{3.25}$$

3.4 Design of folded cascode Op-Amp:

This type is better in terms of performance than the rest of the types, we will process the design of this type and simulate it using the same technology, this type is used in many applications in filters and design of signal amplifiers, etc., Figure (3.5) shows the design for this circuit.[7]

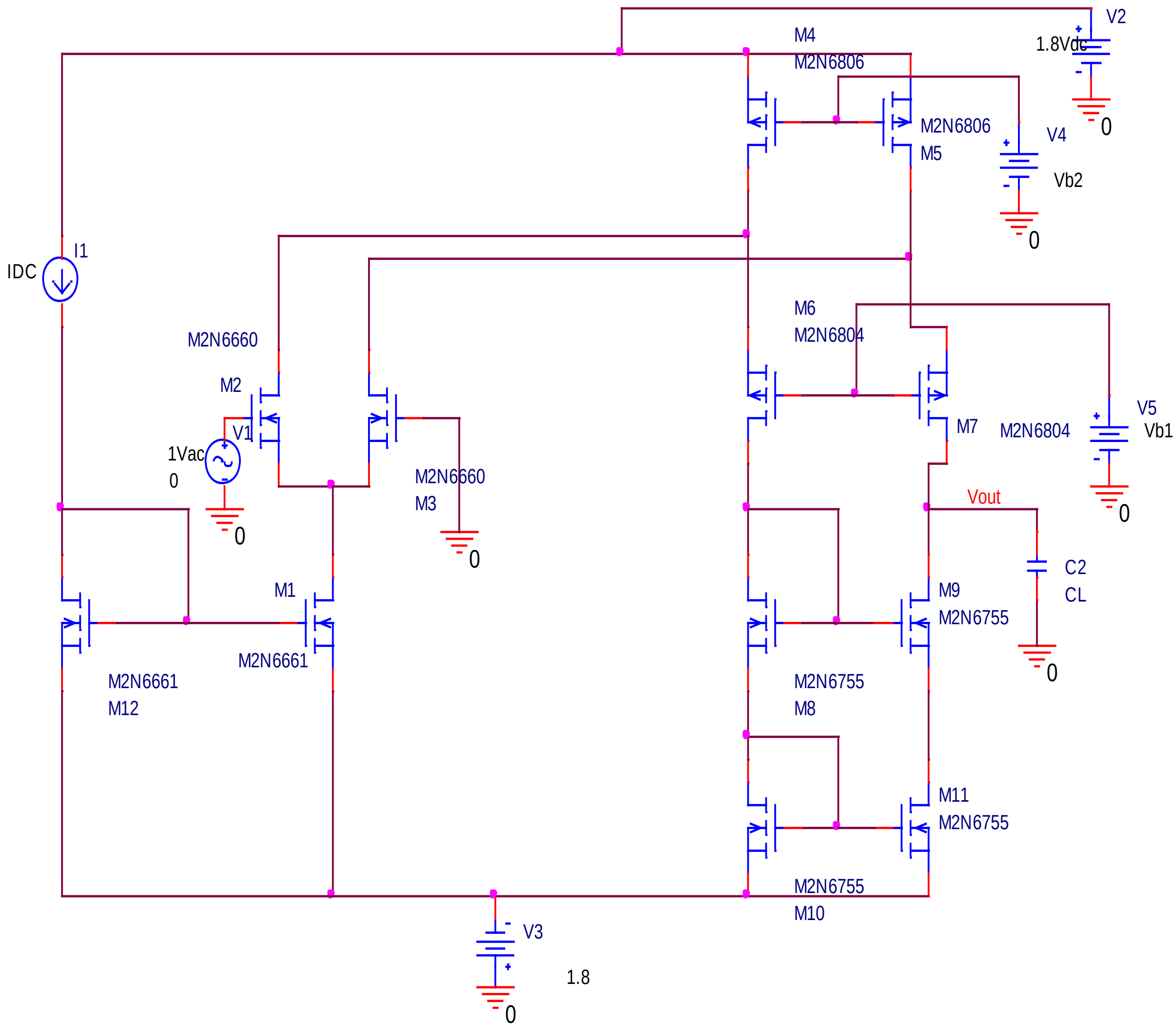


Figure (3.5): Schematic of the folded- cascode of Op-Amp

The amount of the current value in output circuit is very small compared to its value in the input circuit and can be made equal to or close to the input phase in practice, one of the important features in this type is that the bias is self-contained, and the output resistance is high, so the gain in this type is high.

3.4.1 The folded- cascode specifications:

Table (3.4) illustrates the specifications of the folded -cascode op- amp:

Table (3.4): The specifications of self-biased

NO	Specification	Values
1	Gain	>60dB
2	GBW	15MHz
3	(V_{DD},V_{SS})	±1.8V
4	Phase Margin	≥60°
5	Load Capacitor	10pF
6	$\mu_n c_{ox}$	110 μA/V^2
7	$\mu_p c_{ox}$	50 μA/V^2

3.4.2 The equation design of the folded-cascode

The design is according to certain specifications that can be summarized in the Table (3.4), as well as according to the following mathematical equations and relationships from [3.26 – 3.36] [43,44]

The slewrate:

$$I_3 = SR.C_L \tag{3.26}$$

The bias currents:

$$I_4 = I_5 = 1.2I_3 \quad to \quad 1.5I_3 \tag{3.27}$$

$$S_{4,5} = \frac{2I_5}{K_p V_{DS5}^2} \quad (3.28)$$

$$S_{6,7} = \frac{2I_7}{K_p V_{DS7}^2} \quad (3.29)$$

$$S_{10,11} = \frac{2I_{11}}{K_n V_{DS11}^2} \quad (3.30)$$

$$S_{8,9} = \frac{2I_9}{K_n V_{DS9}^2} \quad (3.31)$$

$$GB = \frac{g_{m1}}{C_L} \quad (3.32)$$

$$S_1 = S_2 = \frac{g_{m1}^2}{K_n I_3} = \frac{GB^2 C_L^2}{K_n I_3} \quad (3.33)$$

$$S_3 = \frac{2I_3}{K_n\left[V_{in(min)} - V_{SS} - \sqrt{\frac{I_3}{K_n S_1}} - V_{Tn1}\right]^2} \quad (3.34)$$

$$S_4 = S_5 = \frac{2I_5}{K_p\left[V_{DD} - V_{in(max)} + V_{Tn1}\right]^2} \quad (3.35)$$

$$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{12} + I_{10} + I_{11}) \quad (3.36)$$

3.5 Modification of an operational amplifier using offset cancellation technology

3.5.1 The modification work of the two-stages Op-Amp

The circuit simulation where the method is applied to two designs, the first is the two-stage and other is the telescopic, we extract a value of offset voltage and all other parameter values such as stetting time, phase, gain and others. In the design shown in Figure (4.2), the proposal consists of (M5, M2, M1) where this part represents (G mi), M3and M4 where it represents these two transistors (R1) and the transistors M6 and M7 represent the (A2), as well as representing a group Transistors (M9, M10, M11, M12, M13) the auxiliary amplifier and finally the transistor (M14) represents the (G m, aux).

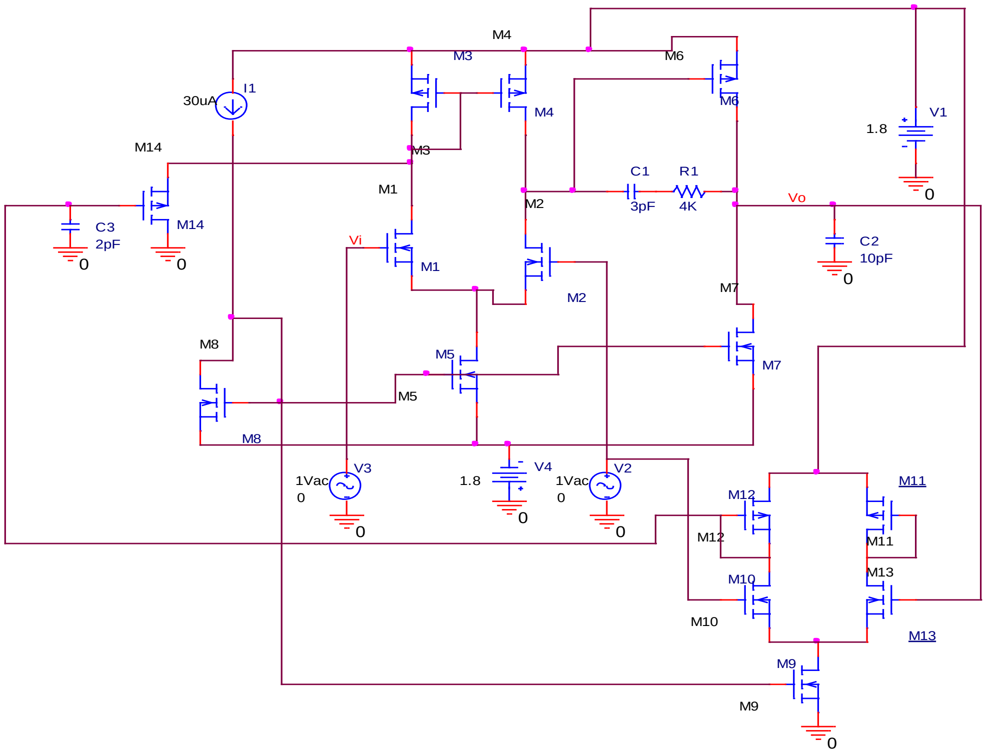


Figure (3.6) Schematic of two-stage modification circuit with cancellation

3.5.2 Proposed of telescopic operation amplifier:

The proposed circuit design for the telescope is shown in the Figure (4.3) the design using orcard P Spice (17 .4)2019 program, where the circuit consists of transistors from (M1-M10) where the design of the telescope and transistors (M11-M15) represents the auxiliary amplifier and finally the transistor (M16) represents the (G m, aux).

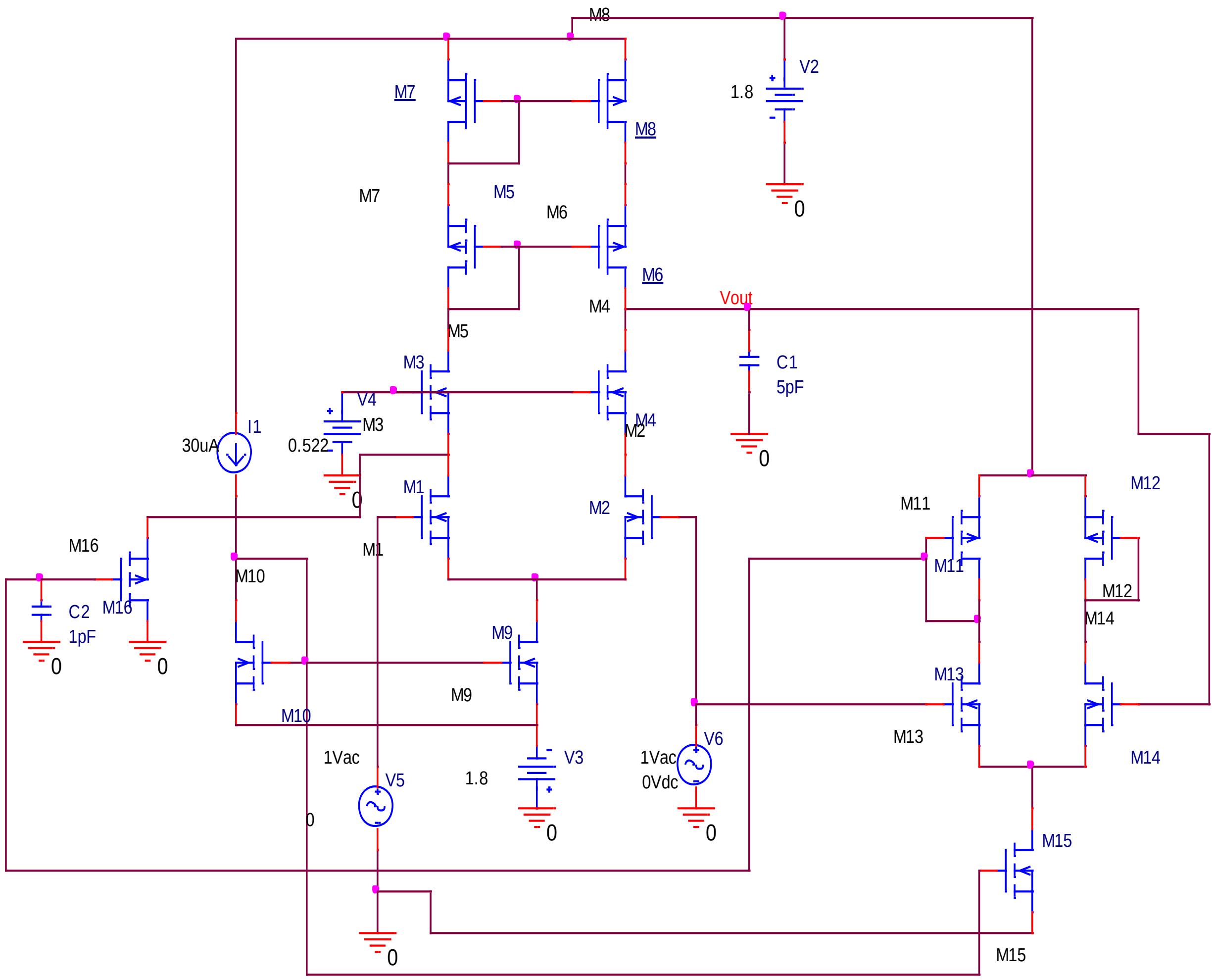


Figure (3.7) Schematic of the proposed circuit of telescopic Op-Amp with cancellation technique

CHAPTER FOUR

Result and discussion

4.1 Introduction:

In this chapter of the thesis, is allocated to results and simulations were devoted to all the designs mentioned previously, where the gain was extracted, gain bandwidth, slew rate, phase margin and settling time, as well as discussing the results of the mentioned designs and knowing the best design in terms of stability, as well as in terms of improvement in terms of offset voltage and others

4.2 Simulation Results:

In this part, the simulation is carried out and the results are presented. The simulation is divided into several parts.

4.2.1 Simulation results of two-stage operational amplifier:

A- Simulation results of the sizes of the Transistors of the two-stage

The final values and results obtained through the design process are indicated in the final Table (3.3).

Table (4.1) The MOSFET ratio (W/L) of two-stages

NO	MOSTET	W/L ratio	W(μm)	L(μm)
1	M1, M 2	3	0.54	0.18
2	M3, M4	15	2.7	0.18
3	M5, M8	4	0.8	0.18
4	M6	94	17	0.18
5	M7	14	2.5	0.18

The above Table shows the width to length ratio of the MOSFET, and this Table was calculated according to the equations.

B- Simulation results of the gain and unity gain band width of the two-stage Op-Amp:

The simulation process of the two-stage circuit extract the gain and gain band width as shown in the Figure (4.1).

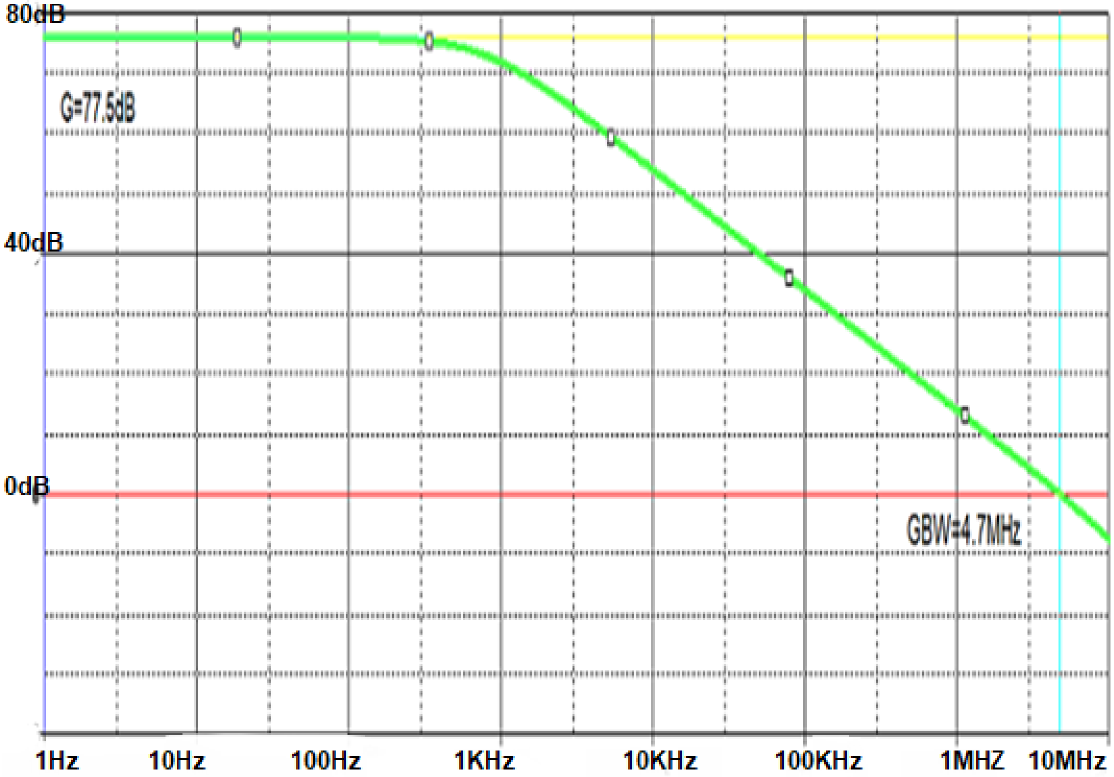


Figure (4.1) Simulation result of two-stage frequency response CMOS Op-Amp

The simulation results, it can be noticed that the gain value is equal to 77.5dB and unity gain band width is 4.7MHz

C- Simulation results of the phase and phase margin of the two-stage Op-Amp

The simulation result of the phase and phase margin of the two-stage Op-Amp shown in Figure (4.2)

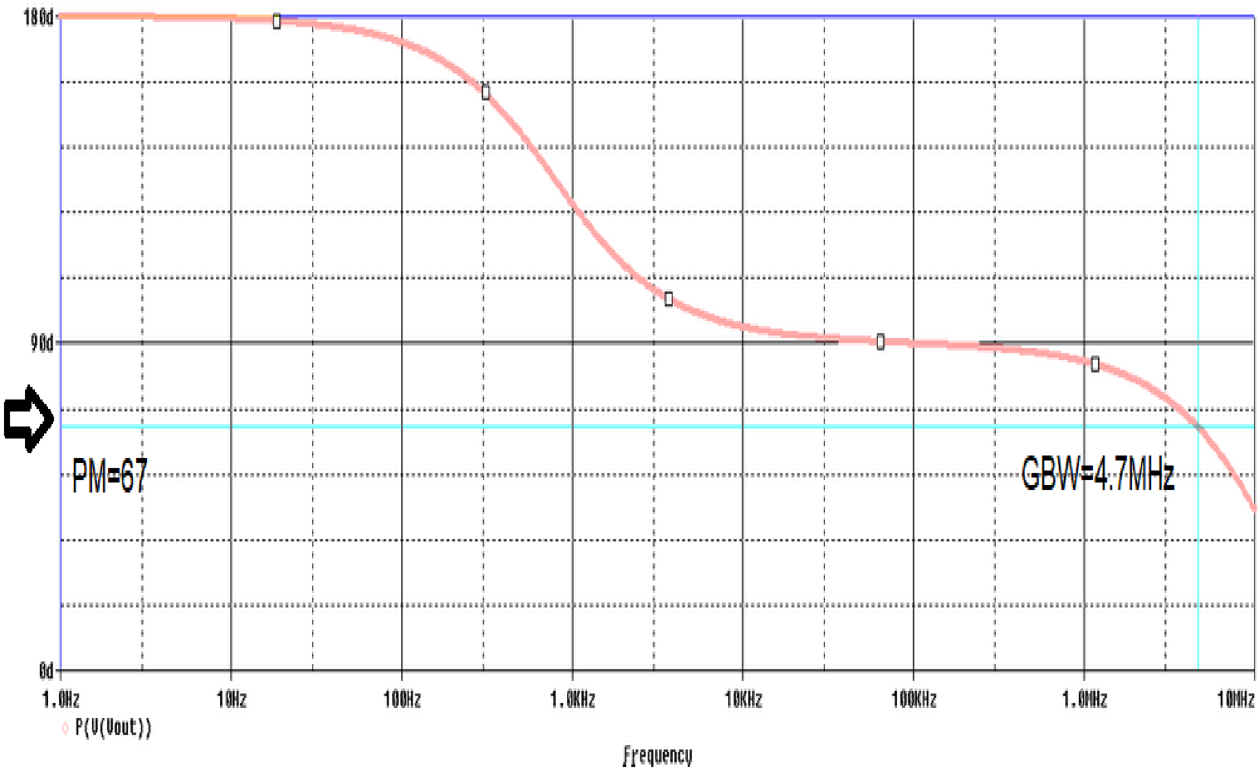


Figure (4.2) Simulation result two-stage frequency response Op-Amp (phase and phase margin)

The Simulation it can be noticed that the phase equal to 180 degree and the phase margin is 67degree, and note that the phase margin is grater thar 45degree that's main the system is stable.

D- Simulation results of the slew rate and settling time of the two-stage Op-Amp:

Simulation result of the circuit to extract slew rate and settling time through the following Figure (4.3) of a two-stage CMOS circuit

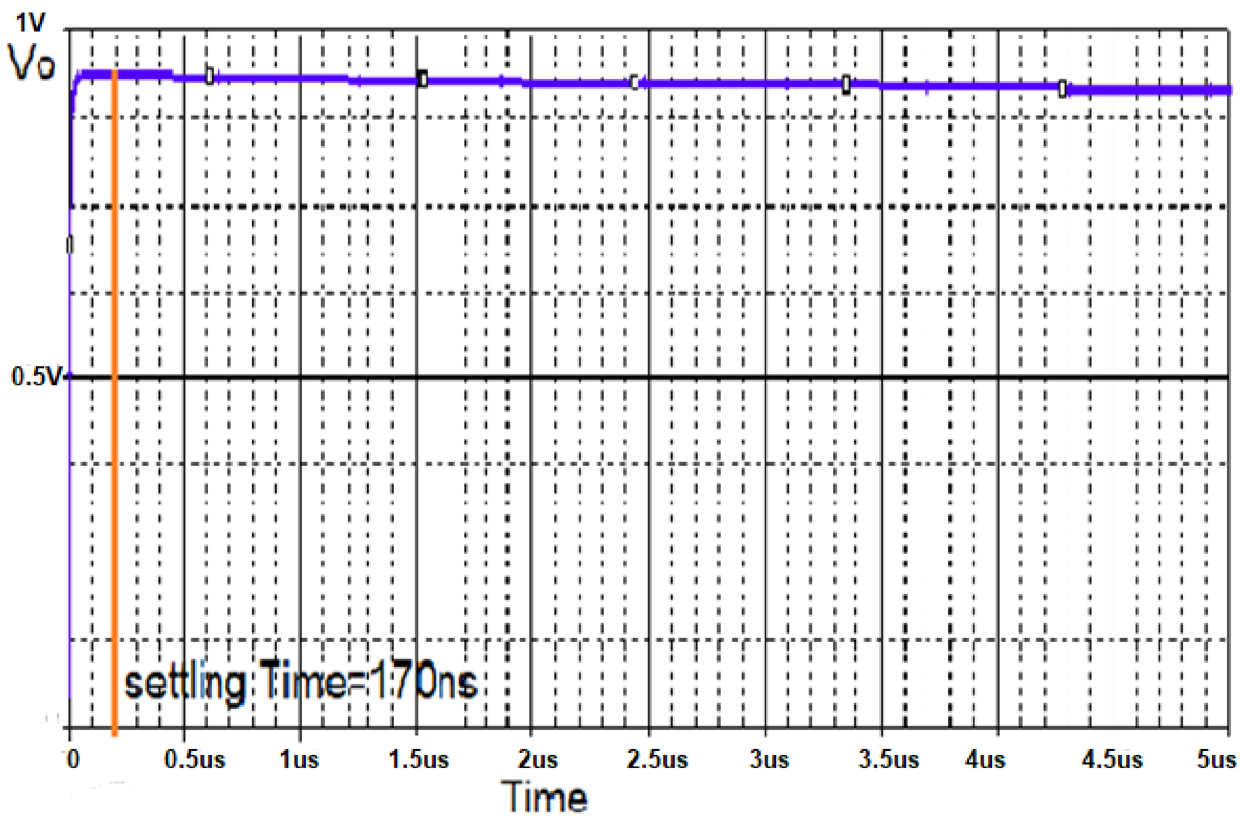


Figure (4.3) Simulation result of two-stage (slew rate and settling time)

The simulation result, it can be noticed that the slew rate of the two -stage is 42 v/µs settling time value is 170ns.

In the below Table show the effect of combination capacitor on the parameter of the circuit two -stage.

Table (4.2) The effect of capacitor (Cl) on the parameter

NO	Gain	phase	GB(MHZ)	Cc(pf)	CL (pf)
1	75	179.97	4.7	3	15
2	75	179.98	4.83	3	10
3	75	179.99	5.1	3	5
4	75	180	5.2	3	1

Table (4.3) The effect of capacitor (Cc) on the parameter

NO	Gain	phase	GB(MHZ)	Cc	CL
1	75	176	1	15	10
2	75	177	1.5	10	10
3	75	178	3	5	10
4	75	180	5	3	10

From Tables nots that the capacitor inversely proportional with unity gain bandwidth and in the first Table the phase is constant as well as in the second the phase inversely proportional with capacitor.

The Table (4.4) shown all parameters results of the design of the two- stage

Table (4.4) The result performance parameters of the proposed of two-stages

NO	Parameters	Value
1	DC Voltage Gain	77.5 dB
2	Gain Bandwidth	4.7 MHz
3	Bias Current	30 µA
4	settling time	170ns
5	Slew rate	42 v/µs
6	Supply Voltage	±1.8V
7	Phase Margin	67°
8	DC Power Dissipation	0.446 mW
9	Offset voltage	71uv

4.2.2 Simulation results of telescopic operational amplifier:

It is known that before any design is made, there must be manual calculations, after which the simulation is performed, in this part, we do the simulation of the circuit to extract the gain, phase, etc., and we will explain it in several points and the technology used for the design is 180 nm, according to the Table (3.1)

A- Simulation results of the sizes of the transistors of the telescopic:

The final values and results obtained through the design process are indicated in the final Table (4.5).

Table (4.5): MOSFET ratio and width of all transistor.

No	Transistors	W(µm)	L(µm)
1	M_1, M_2	1.3	0.18
2	M_3, M_4	2.6	0.18
3	M 5, M 6, M 7, M 8	2	0.18
4	M 9, M 10	0.8	0.18

B- Simulation results of the gain and unity gain band width of the telescopic Op-Amp

Simulation process of the telescope circuit of the frequency response to extract the gain and bandwidth as shown in the Figure (4.4).

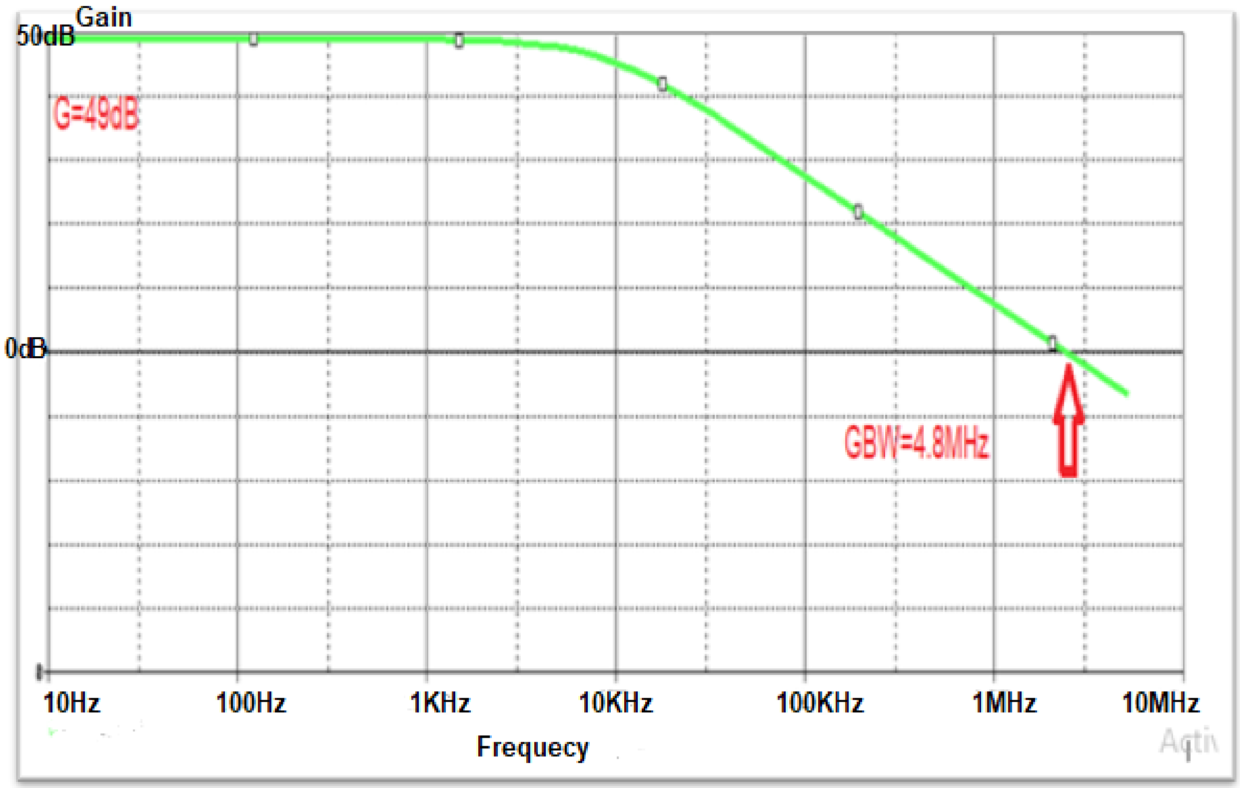


Figure (4.4) The telescopic gain and gain bandwidth.

The frequency response is shown in the Figure (4.4), the gain of the voltage value (49 dB) and the unity gain bandwidth value for this design is equal to (4.8 MHz).

C- Simulation results of the phase and phase margin of the telescopic Op-Amp:

Simulation process of the telescope circuit of the frequency response to extract the phase and phase margin as shown in the Figure (4.5).

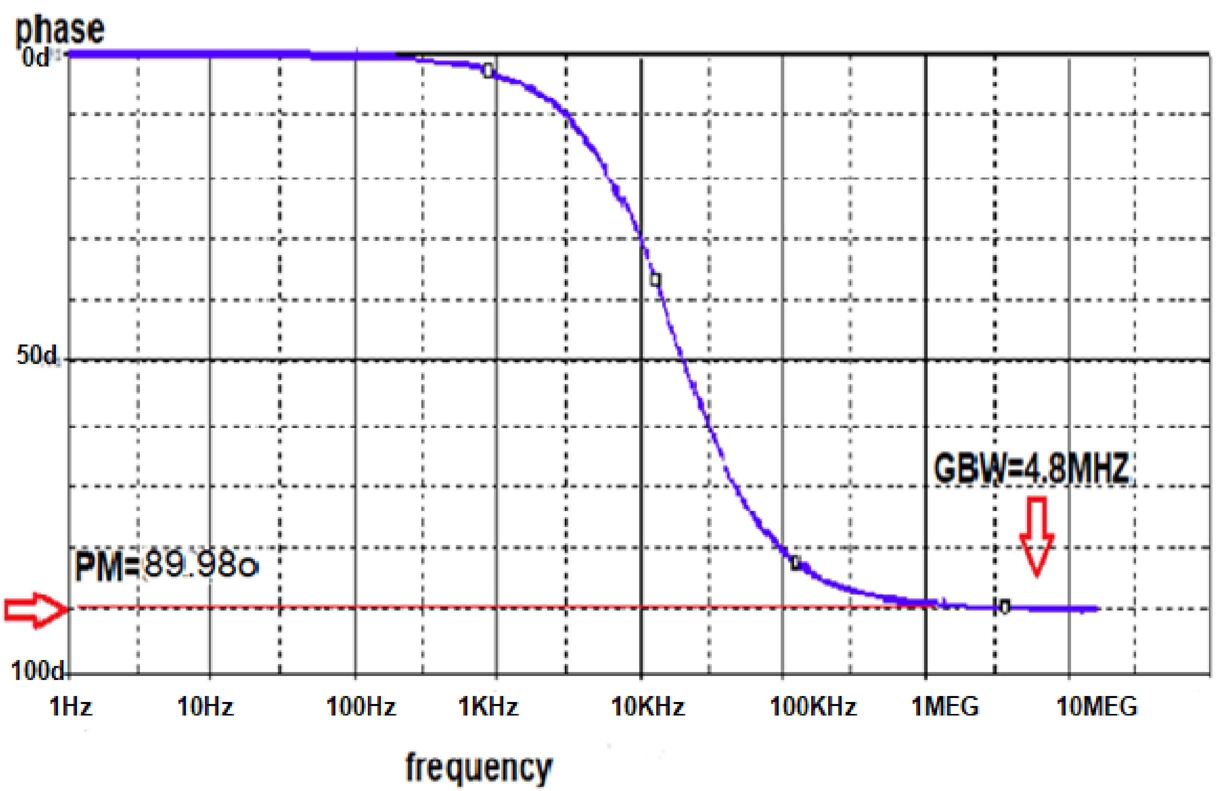


Figure (4.5) The phase (shift and margin) of telescopic

The simulation results of the design show that the phase margin value is 89.98

D- Simulation results of the slew rate and settling time of the telescopic Op-Amp:

The simulation result of the circuit to extract slew rate and settling time through the following Figure (4.6).

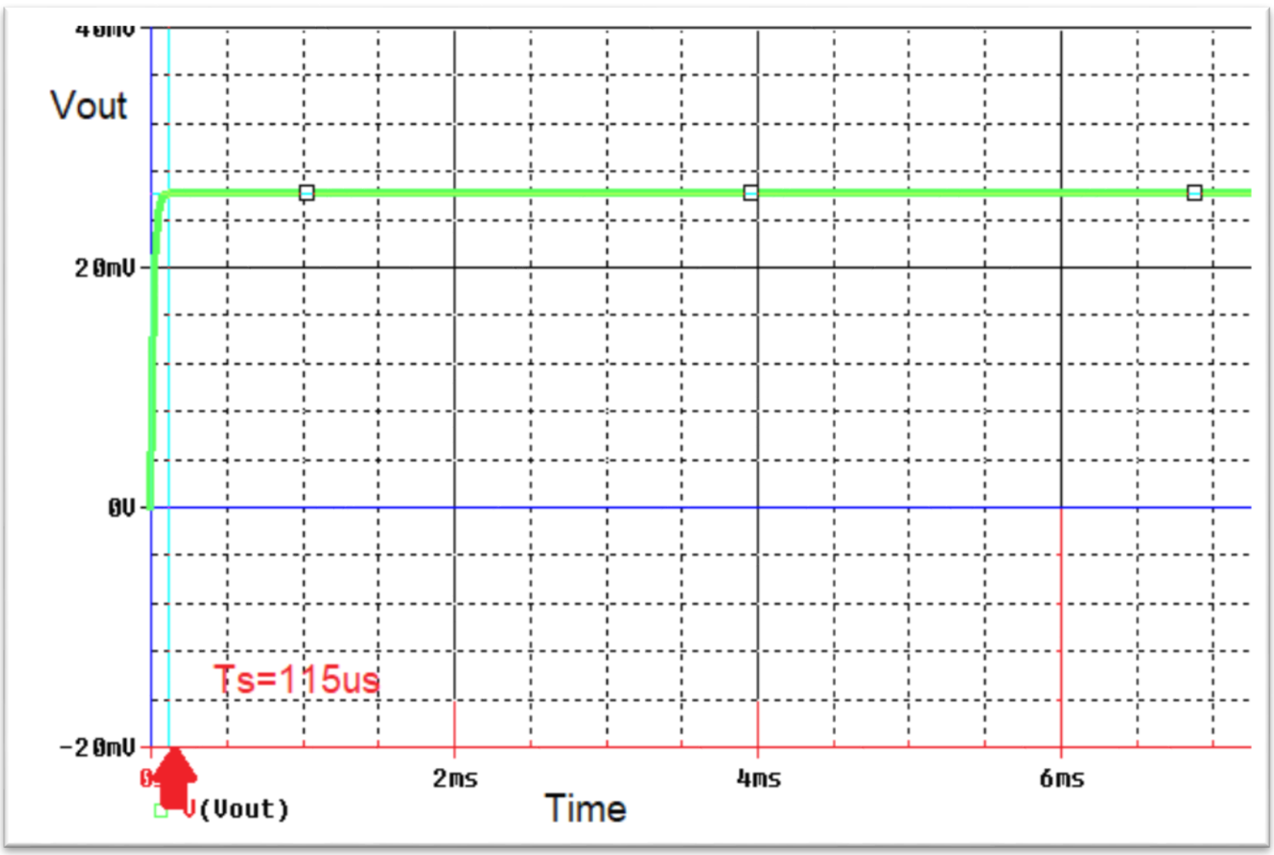


Figure (4.6) Telescopic slew rate and settling time

The simulation result, notices that the slew rate of the telescopic is 8.7 v/µs , settling time value is 115µs.

The following Table (4.6) shows the effect of load capacitor on some circuit parameter where we will take its effect on gain, phase margin and unity-gain bandwidth.

Table (4.6) The effect of capacitor (Cl) on the parameter

CL (pf)	UGB(MHZ)	PM (degree)	Av(dB)
1	12	89.9	49
2	11.9	89.92	49
3	8	89.94	49
4	6	89.96	49
5	4.8	89.98	49
6	4	89.99	49
7	3.4	89.991	49
8	3	89.995	49
9	2.6	90	49
10	2.4	90.1	49

From the result obtained in the Table (4.6) see that the unity-gain bandwidth (UGB) is inversely proportional with the load capacitor (CL) While the phase margin (PM) is proportional with the load capacitor and the Gain stay constant and does not affect

The Table (4.7) shown all parameters results of the design of the two- stage

Table (4.7) Suggested Op-Amp telescopic CMOS parameters.

NO	Parameters	Value
1	Gain	49 dB
2	GBW	4.8 MHz
3	Ib	30 µA
4	settling time	68µs
5	Slew rate	8.7 V/µs
6	Supply Voltage	±1.8 V
7	Phase Margin	89.98°
8	DC Power Dissipation	0.164 mW
9	Offset voltage	26mv

4.2.3 Simulation results of folded-cascode operational amplifier:

A- Simulation results of the sizes of the transistors of the folded-cascode:

The following Table (4.8) shows the values of the sizes of the transistors in the design, which are the same as the values used in the program.

Table (4.8) The transistor ratio of folded-cascode.

NO	Transistor number	Gate width (μm)	Channel length (μm)
1	M_2, M_3	22	0.18
2	M_4 , M_5	3	0.18
3	M_6 , M_7	5.4	0.18
5	M_8 , M_9 , M_{10} , M_{11}	6	0.18
6	M_{12} ,M1	0.4	0.18

B- Simulation results of the gain and unity gain band width of the folded-cascode Op-Amp:

Simulation process of the folded-cascode Op-Amp circuit of the frequency response to extract the gain and bandwidth as shown in Figure (4.7).

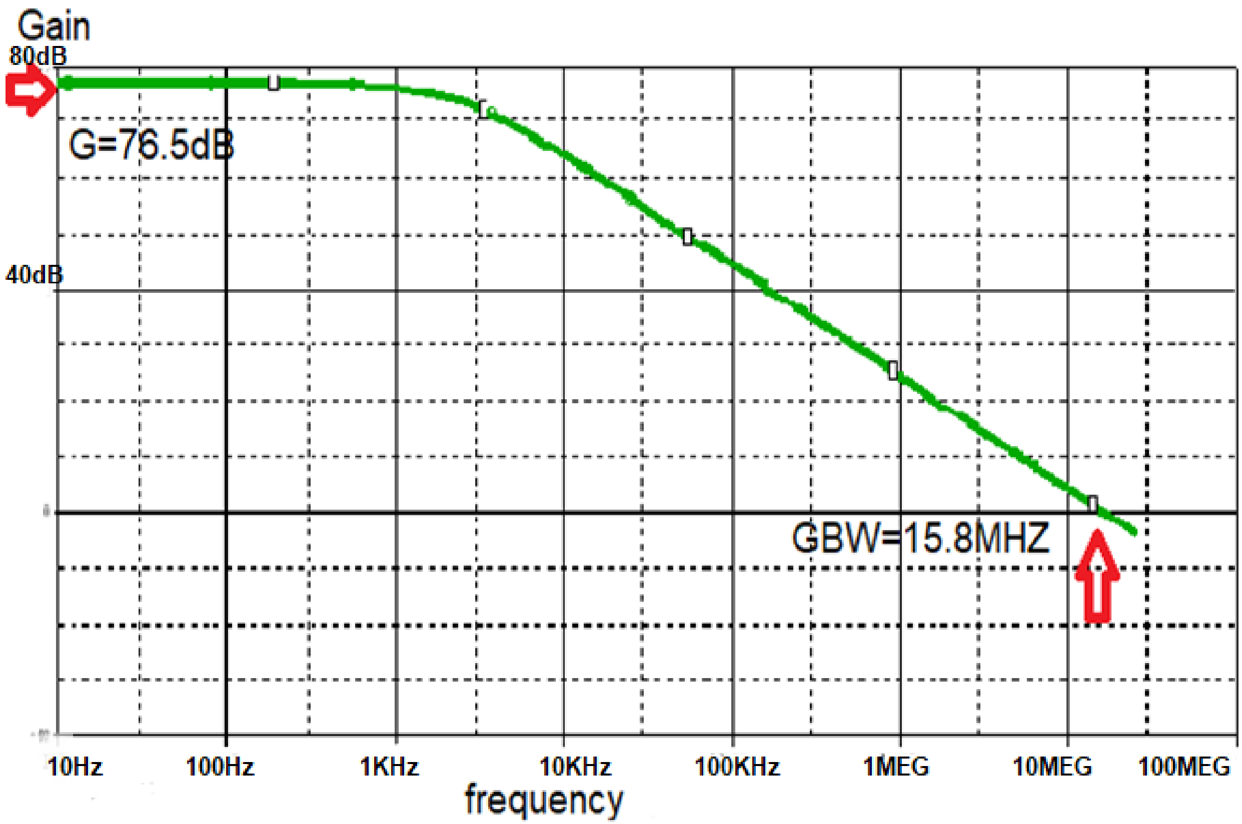


Figure (4.7) The folded-cascode (gain) and gain bandwidth.

The frequency response is shown in Figure above, the gain of the voltage value (76.5dB) and the unity gain bandwidth value for this design is equal to (15.8MHZ)

C- Simulation results of the phase and phase margin of the folded-cascode Op-Amp:

Simulation process of the folded-cascode Op-Amp circuit of the frequency response to extract the phase and phase margin is shown in the Figure (4.8).

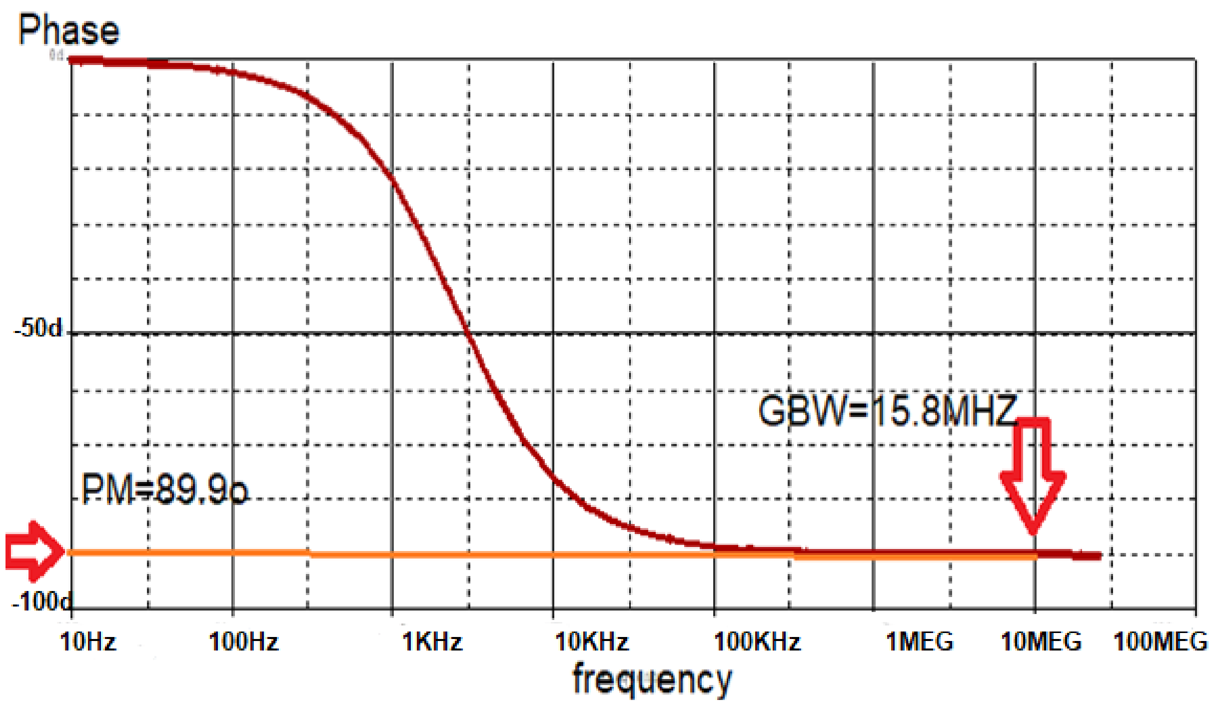


Figure (4.8) The Phase (Shift and margin) of folded-cascode

The simulation results of the design show that the phase margin value is 89.9

D- Simulation results of the slew rate and settling time of the folded-cascode Op-Amp

The simulation result of the circuit to extract slew rate and settling time through the following Figure (4.9).

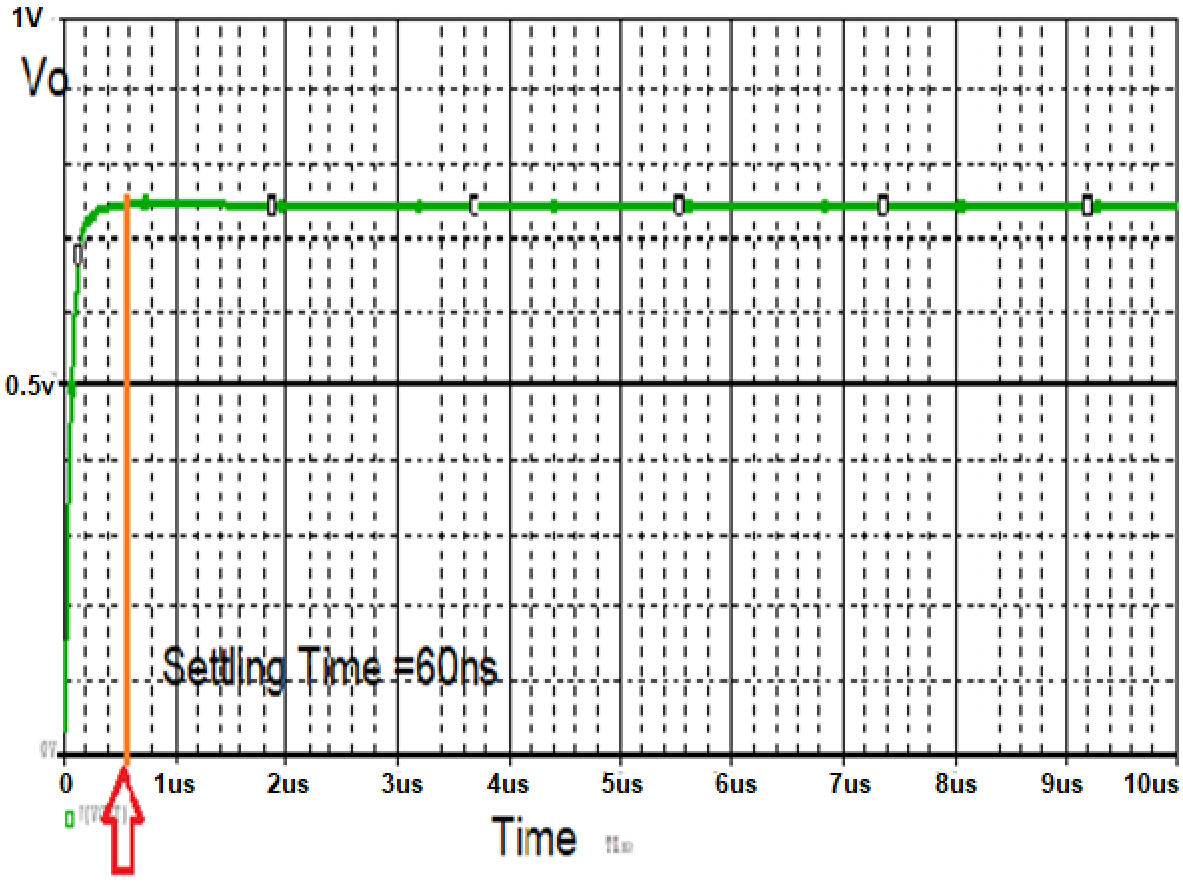


Figure (4.9) Folded slew rate and settling time

The simulation result, it noticed that the slew rate of the folded-cascode is 12 v/µs , settling time value is 60ns.

Table (4.9) Performance folded-cascode Op-Amp

NO	Parameters	Value
1	Gain	76.5 dB
2	GBW	15.8 MHz
3	Ib	30 µA
4	Supply Voltage	±1.8 V
5	PM	89.9˚
6	DC Power Dissipation	0.82 mW
7	settling time	60 ns
8	Slew rate	12 V/µs
9	Offset voltage	8.6mv

4.3 Simulation result modification and proposed with cancellation:

In this part of the thesis, the results of the modified design as well as the proposed design are discussed, a comparison with previous studies is made, and the improvements obtained from the designs are recognized.

4.3.1 Simulation result of proposed two-stage with cancellation:

The simulation result of the design of the two -stage it can be made on several points where these points form the size of the transistors, gain, phase, phase margin, and others.

A- Simulation results of the sizes of the transistors of the two -stage:

In this part of the research, the same previous equations will be used in the two-stage circuit, the design was made with a technique of 180 nm and a voltage source of 1.8 volts the designed by P-Spice 17.4 software, where the sizes of the transistors were as in the following Table (4.10)

Table (4.10) the ratio of ($\frac{W}{L}$) proposed of two stages CMOS with cancellation technique

NO	MOSTET	W/L ratio	Width(W)(μm)	Length(L)(μm)
1	M1, M2	3	0.54	0.18
2	M3,M4	15	2.7	0.18
3	M5,M8	4.4	0.8	0.18
4	M6	94	17	0.18
5	M7	14	2.5	0.18
6	M9	3	0.54	0.18
7	M10, M11	94	17	0.18
8	M12, M13	14	2.5	0.18
9	M14	4	0.72	0.18

B- Simulation results of the gain and gain bandwidth of the transistors of the two-stags:

The simulation process of the two-stage circuit extract the gain and gain band width as shown in the Figure (4.10) below.

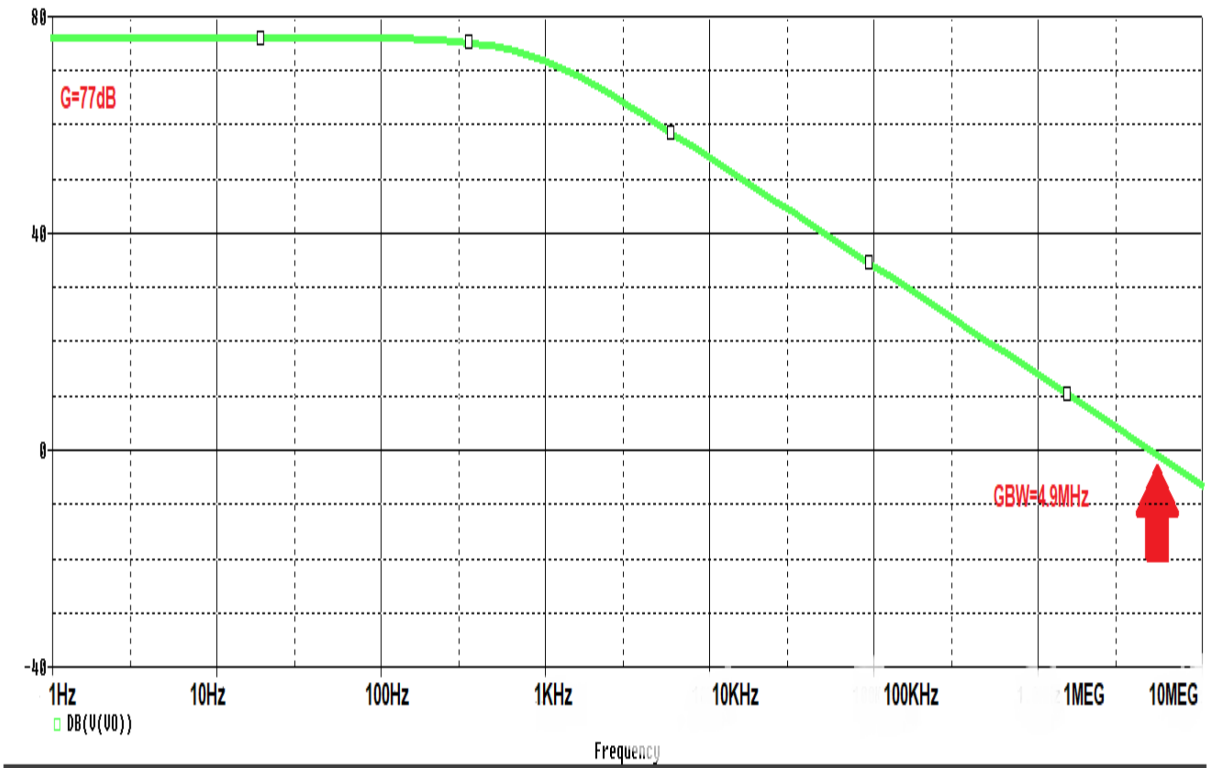


Figure (4.10) Simulation result of the two-stage frequency response CMOS with cancellation technique (gain , gain bandwidth)

The simulation it noticed that gain value is equal to 77dB and unity gain band width is 4.9MHz

C- Simulation results of the phase and phase margin of the transistors of the two-stags:

The simulation of phase and phase margin of a two- stage CMOS circuit shown in Figure (4.11)

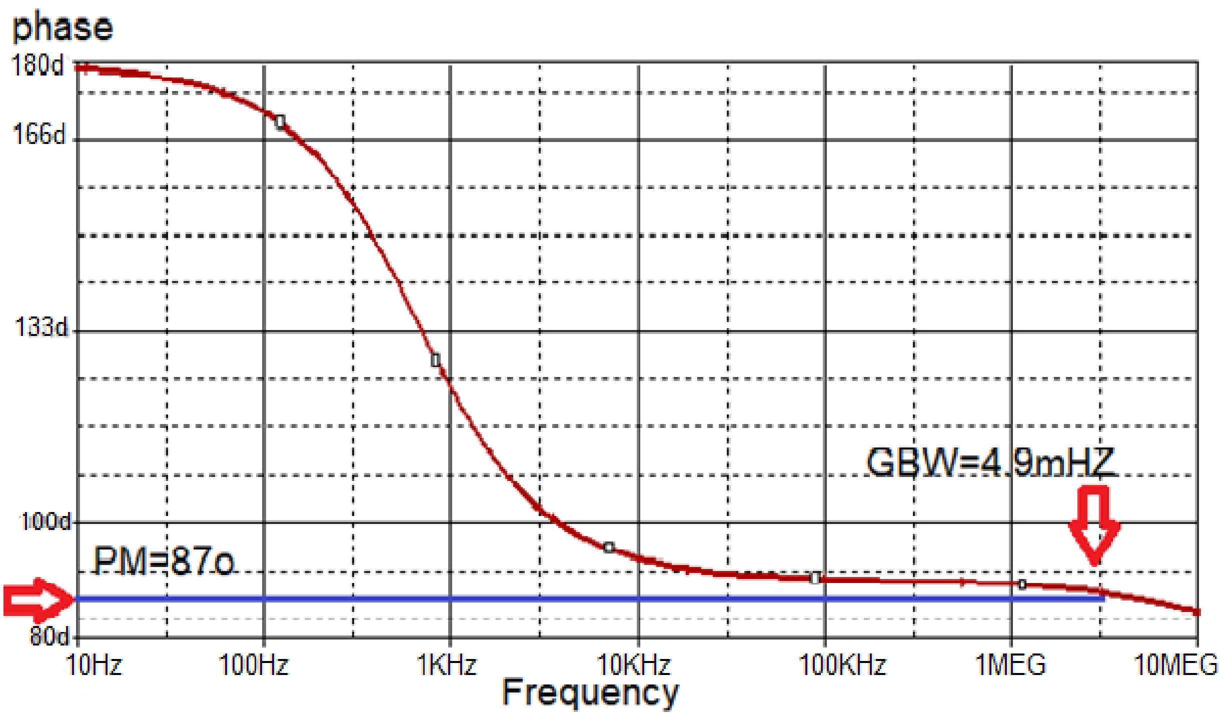


Figure (4.11) Simulation result of two-stage frequency response with cancellation (phase, phase margin)

The simulation, it notice that the phase equal to 180degree and the phase margin is 87 degree, and note that the phase margin is grater thar 45 degree that's main the system is stable.

D- Simulation results of the slew rate and settling time of the Two-stage:

Simulation of the circuit to extract slew rate and settling time through the following Figure (4.12) of a two-stage CMOS circuit with cancellation technique

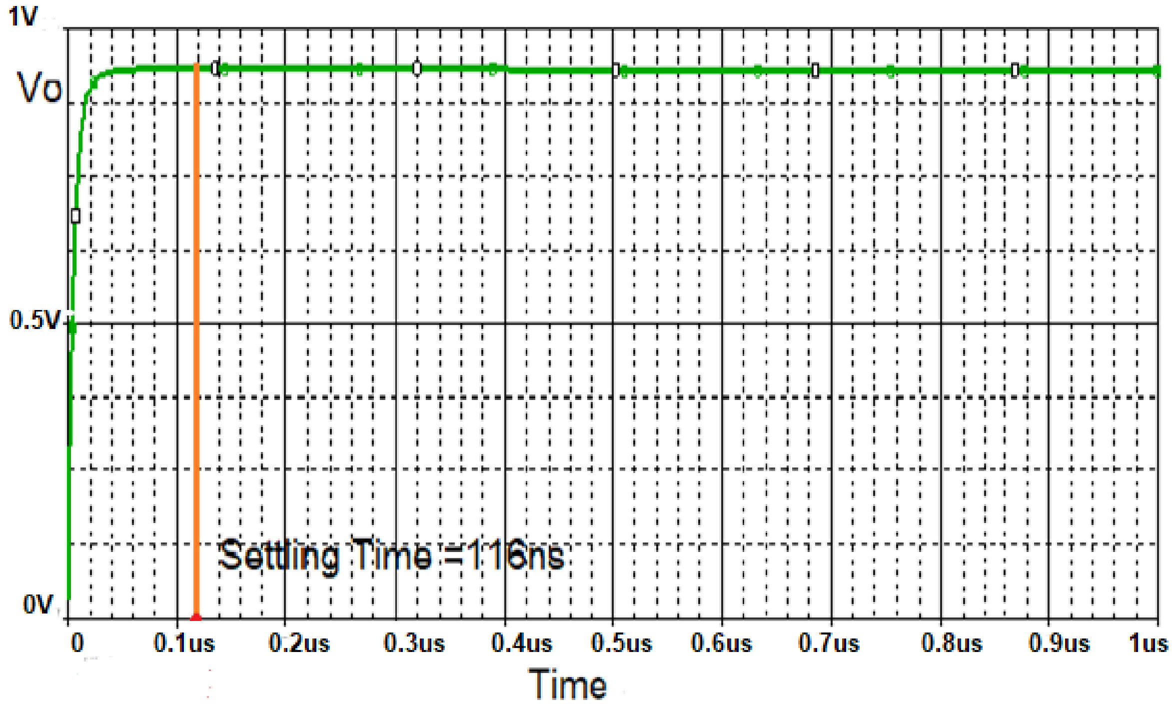


Figure (4.12) Simulation result of two-stage CMOS Op-Amp with cancellation technique (slew rate and settling time)

The simulation result of the time domain or transient shows that the settling time is 116 ns and the slew rate is 42 v/µs

4.3.2 Results of the proposed telescopic CMOS Op-Amp with cancellation technique:

The simulation and results of the design of the telescopic CMOS Op-Amp it can be made on several points where these points form the size of the transistors, gain, phase, phase margin, and others.

A- Simulation results of the sizes of the transistors of the telescopic:

In this part the design was made with a technique of 180 nm and a voltage source of 1.8V the designed by P-spice 17.4 software, where the sizes of the transistors were as in the following Table (4.11)

Table (4.11) The ratio of ($\frac{W}{L}$) proposed of telescopic CMOS with cancellation technique

NO	MOSTET	W/L ratio	Width(W)(μm)	Length(L)(μm)
1	M1, M 2	7	1.3	0.18
2	M 3, M 4	14	2.6	0.18
3	M 5- M 6 M 7- M 8	4.4	0.8	0.18
4	M9-M10	4.4	0.8	0.18
5	M15	3	0.54	0.18
6	M13-M14	94	17	0.18
7	M11- M11	14	2.5	0.18
8	M16	4.4	0.8	0.18

B- Simulation results of the gain and gain bandwidth of the transistors of telescopic:

Through the simulation process of the circuit in the case of the IC, and through it, we extract the gain and gain bandwidth, as in the Figure (4.13) below.

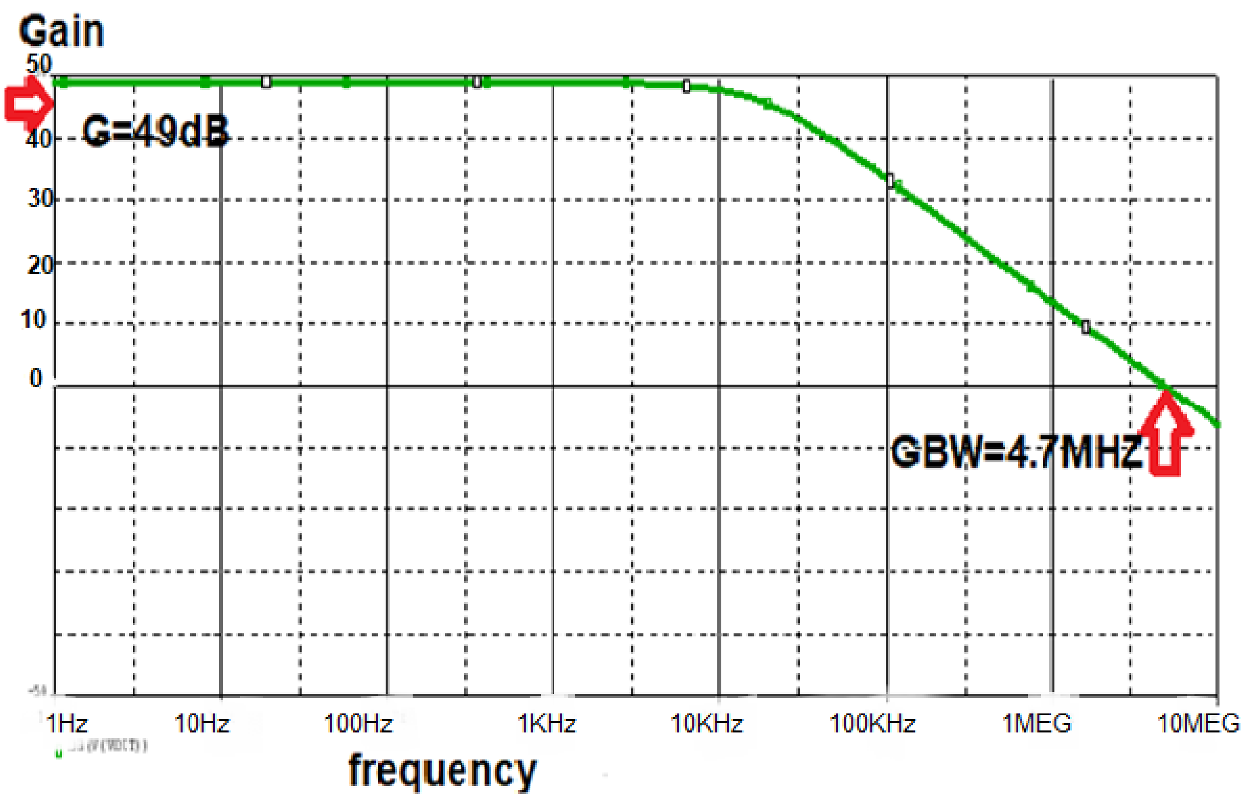


Figure (4.13) Simulation result of the telescopic frequency response CMOS with cancellation technique (gain , gain bandwidth)

The simulation, it noticed that the gain value is equal to 49dB and unity gain band width is 4.7MHZ

C- Simulation results of the phase and phase margin of the transistors of the telescopic:

The simulation of phase and phase margin of telescopic circuit in Figure (4.14)

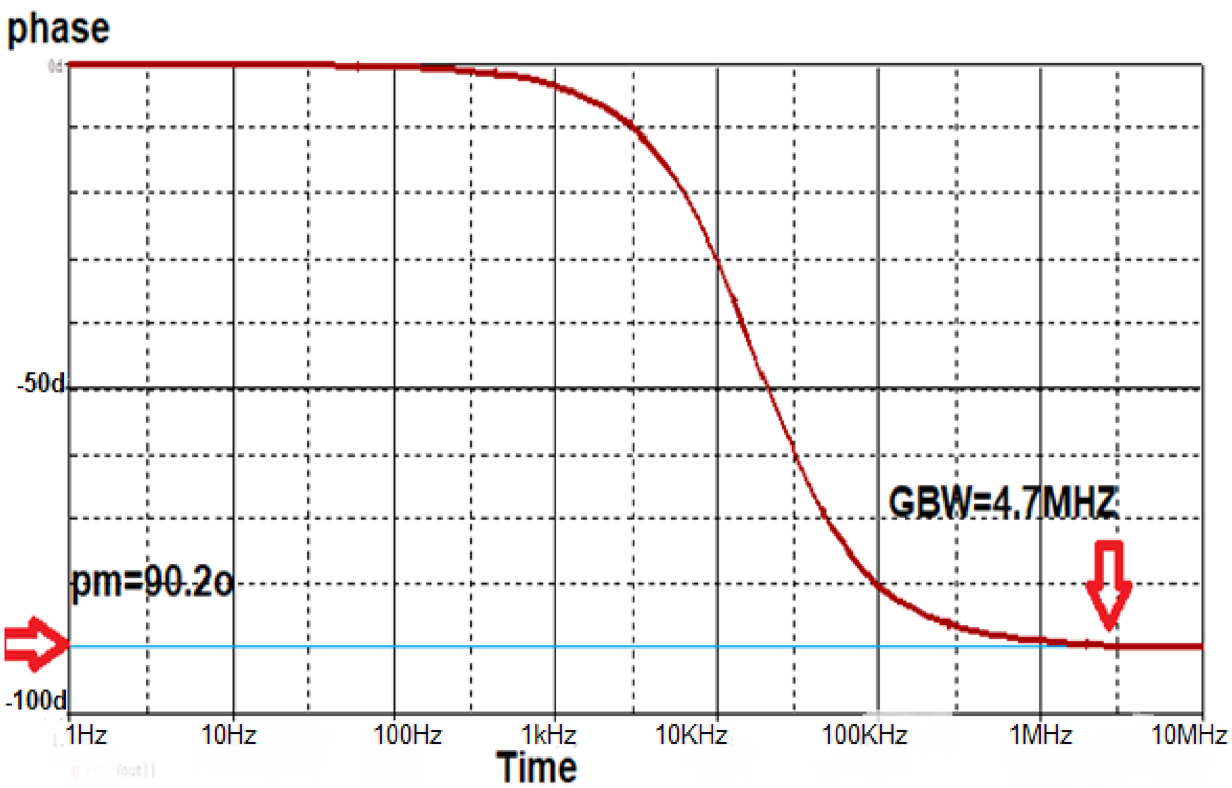


Figure (4.14) Simulation result of the telescopic frequency response CMOS with cancellation technique (phase , phase margin)

The simulation, it noticed that the phase margin is 90.2 degree, and note that the phase margin is grater thar 45 degree that’s main the system is stable

D- Simulation results of the slew rate and settling time of the telescopic:

Simulation of the circuit to extract slew rate and settling time through the following Figure (4.15) of a telescopic CMOS circuit with cancellation technique.

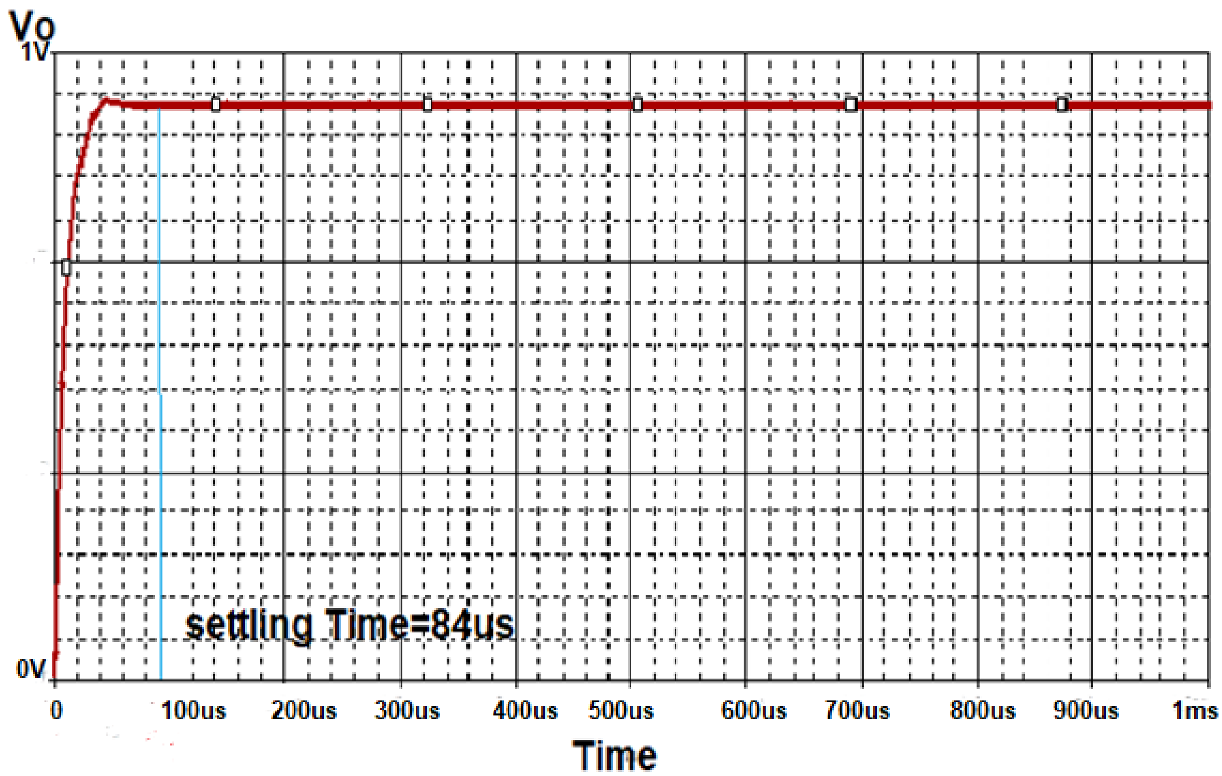


Figure (4.15) Simulation result of telescopic CMOS Op-Amp with cancellation technique (slew rate and settling time)

The simulation result of the time domain or transient shows that the settling time is 84 µs and the slew rate is 4.6 v/µs

4.4 General performance parameters of the proposed design:

In the following Table (4.12) and Table (4.13) the simulation results and the resulting properties of the proposed circuit

Table (4.12) The result of the proposed of Two stages CMOS with cancellation technique

No	Parameter	Value
1	Power supply	±1.8V
2	Gain	77dB
3	Phase	180˚
4	Gain bandwidth	4.9 MHz
5	Phase margin	87
6	Offset Voltage	21µV
7	Power dissipated	0.4mw

Table (4.13) The result of the proposed of Telescopic CMOS with cancellation technique

No	Parameter	Value
1	Power supply	±1.8V
2	Gain	49dB
4	Gain bandwidth	4.7 MHZ
5	Phase margin	90.2
6	Offset Voltage	1.3mV
7	Power dissipated	0.16MW

The Simulation Results of the both design through the final results, an observation of the value of the offset voltage of the first design is equal to 21 µV and the percentage of improvement over the first design is 70%. The second design is the telescopic the value of the offset voltage 10 mV and the percentage of improvement 94%.

4.5 Comparison of the proposed design and the previous works design:

In order to know which designs are the best, there must be a comparison between them. In the following Table, a comparison between the proposed design and the previous design, where the results show that the proposed design is better in several points.

Table (4.14) Comparison between the proposed work and related previous works

NO	parameter	Proposed work	[51-2007]	[25-2017]	[28-2019]	[30-2020]
1	Technology	180nm	350nm	180nm	40nm	180nm
2	Power supply	±1.8V	3.3V	±1.8V	1.1V	1.8V
3	gain	77dB	-	11.5dB	21.26 dB	-
4	Offset Voltage	21 µV	1.898mV	52.58mV	14.41mV	6mV
5	Power dissipated	0.4mw	0.6mW	-	-	4.72µW
6	Phase margin	87		89	45◦	-

The simulation results in progress and improvement in the value of the offset voltage when comparing the design results with those of previous years.

4.6 MOSFET chip area:

To manufacture the transistor and know the total area of the design can be done through the following equation

$$Area\ of\ MOS = \sum_{1}^{n} W_i L_i$$

$n = number\ of\ mosfet\ in\ circuit$

Table (4.15) The MOSFET areas

OP-AMP	**Area**
Two- stage	4.9644 μm^2
Telescopic	3.132 μm^2
Folded-cascode	11.1132 μm^2
Two-stage with cancelation	12.2112 μm^2
Telescopic with cancelation	10.3788 μm^2

From the above table notes that the area of the telescopic is less one (3.132 μm^2) ,the two-stage is greater than telescopic (4.9644 μm^2) and the folded cascode is greater than both two design (11.1132 μm^2).The two-stage with cancelation is (12.2112 μm^2) and telescopic with cancelation is (10.3788 μm^2) .The area depends on the number of transistors and the width and length of each transistor.

4.7 comparison between the all design of Op-Amp:

In the following Table (4.16), it shows the most important characteristics and the parameter between the three proposed designs, where we summarize in it the whole parameter that affects the three designs

Table (4.16) Parameters all MOS FET.

NO	PARAMETERS	TWO - STAGE	TELESCOPIC	FOLDED-CASCOD	TWO - STAGE with cancelation	TELESCOPIC With cancelation
1	DC Gain	77.5dB	49 dB	76.5 dB	77dB	49dB
2	Gain bandwidth (GBW)	4.7 MHz	4.8MHz	15.8 MHz	4.9 MHz	4.7 MHz
3	Bias current (IB)	30 µA	30 µA	30 µA	30 µA	30 µA
4	Supply voltage (VDD,VSS)	±1.8 V	±1.8 V	±1.8 V	±1.8 V	±1.8 V
5	Phase margin	67∘	90.2∘	89.9∘	87	90.2
6	Slew rate	42 V/µs	8.6 V/µs	12 V/µs	42 v/µs	4.6 v/µs
7	Settling time (Ts)	170 ns	115 µs	60 ns	116 ns	84 µs
8	Chip area	4.9644 μm^2	3.132 μm^2	11.1132 μm^2	12.2112µm2	10.3788 μm^2
9	DC Power dissipation	0.446mW	0.164 mW	0.82 mW	0.4mW	0.16MW