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Performance Analysis and Evaluation of Different Voltage Balancing Schemes for a Grid Connected Modular Multilevel Converter under Asymmetrical Grid Condition

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Abstract: Furnished with many features, modular multi-level converters (MMC) have various applications in power systems. The main application considered is high voltage direct current transmission (HVDC), where the MMC operates as back to back converters. In this work, an MMC is studied as an interfacing converter, between a distributed energy source and an unbalanced grid. Therefore, at the point of common coupling (PCC) the voltage and current is a composite of positive, negative and zero sequence components. A mathematical relationship for the MMC arm current is developed that accounts for the presence of the PCC voltage and current zero sequence in addition to the positive and negative components. Since current is injected towards the grid, the profile of the converter output voltage is an important factor. This voltage is implicitly affected by the sub-module capacitor voltage; hence, the balancing scheme adopted is pivotal in grid connected applications. Therefore, two balancing techniques are investigated, where one depends on simply rotating the carriers between sub-modules of the MMC. The other is based on the conventional sorting algorithm. Results show that the former method, which requires less calculation efforts, provides sufficient results in-terms of the current shape and ripple injected by the converter compared to the sorting based benchmark scheme. This is attributed to the converter output voltage, for which simulation results confirm that the rotation method contributes to small deviations in this voltage. Evaluations of balancing methods presented in this work prove that the rotation method is a sufficient balancing platform for interfacing MMC applications.

Keywords: Modular multilevel converters, Voltage balancing schemes, Point of common coupling, Symmetrical components.

List of Notations

i_{pccy}: Instantaneous current at PCC for phase y.
i_{uy}: Instantaneous upper arm current for phase y.
i_{ly}: Instantaneous lower arm current for phase y.
i_{cy}: Instantaneous circulating current per converter leg (phase).
i_{cda}: Average value of circulating current for phase *a* of the converter.
i_{uy}^{dc}: DC component of upper arm current for phase y.
i_{uy}^{0}: Zero sequence component of upper arm current for phase y.
$i_{uy}^{1(2)}$: Positive (negative) sequence component of upper arm current for phase y.
I_{cna}: Peak current for n[th] harmonic component of circulating current for phase *a*.
I_{pcc}^{012}: Zero, positive or negative component of PCC current.
N: Number of sub-modules in a converter leg.
N_u: Number of sub-modules in an upper arm of a converter leg.
N_l: Number of sub-modules in the lower arm of a converter leg.
V_{aO}: Converter output voltage relative to mid-point O for phase *a*.
V_{Dc}: Rated voltage of DC side.
v_{pccy}: Instantaneous voltage at PCC for phase y.
V_{pcc}^{012}: Zero, positive or negative component of PCC voltage.

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δ_n: Phase angle for the n[th] frequency circulating current component.
$\theta^0_{v(i)}$: Angle of zero sequence PCC voltage (current) component.
$\theta^1_{v(i)}$: Angle of positive sequence PCC voltage (current) component.
$\theta^2_{v(i)}$: Angle of negative sequence PCC voltage (current) component.

1. Introduction

Compared to other converters, the modular multilevel topology presents several potentials that can provide enhancement and flexibility in power system applications. These potentials include, a high voltage output that closely mimics a much desired sinusoidal variation, expandability and only a single energy source is required [1, 2]. The topology pioneered by [3] proved itself as a high profile competitor compared to other high voltage topologies such as a string of two level converters. The building block of the MMC is either a half or full bridge two level topology in addition to a capacitor. Each block is referred to as a sub- module. The capacitor voltage tends to deviate from the typical value and this calls for an integral balancing action [4]. Existing literature have dealt with circulating current suppression [5-7] and balancing voltage across individual capacitors [8-11]. Balancing the voltage across sub-module capacitors has been implemented by the sorting method presented in [8], where the voltage magnitudes are arranged in ascending and descending order, depending on information from the PWM, a sub-module with highest/lowest capacitor voltage is inserted /bypassed depending on whether the arm current is positive or negative. To eliminate the need of current sign detection, authors in [9] proposed an alternative method to determine whether the sub-module capacitors are charging or discharging. This method is based on determining the sign of the rate of change of total capacitance voltage per arm, where a positive sign indicates a charging status and vice versa. Authors report that this would reduce control requirements and achieves a low cost version of the conventional sorting method. An approach to alleviate the amount of switching actions, which occur in conventional sorting method, is presented in [10]. The goal is to maintain conducting sub-modules status in a future switching period. First, through the capacitor voltage measurements, the conducting sub-modules are isolated from non-conducting (or bypassed) ones. Authors proposed an isolation process implemented by offsetting the voltage measurements by an amount which depends on the switching status. If the voltage level requires the same number of conducting sub-modules, the balancing algorithm keeps the same sub-modules, whereas an increase or decrease in level results in connecting or bypassing sub-modules according to the sorting list. This method, however still requires sign detection of arm current and measurements of all capacitor voltages in the leg of a converter. To remove the sorting process, an approach which is based on comparison of capacitor voltage is presented in [11]. This approach compares normalized voltage values of sub-modules capacitors and a virtual voltage index is established. Another index is mathematically determined which is based on whether the arm current is charging or discharging the capacitor. Hence this method also requires the determination of the sign of arm current as part of the operation.

Beside drive based applications [12], MMC has been used in high voltage DC/AC-transformer system [13] and (HVDC) transmission due to its high voltage capability for conditions where the AC system is enduring an unsymmetrical fault, leading to unbalanced voltage [14-18].

In [13] a method is presented to control the circulating current during a fault on the AC grid which the MMC is connected to. Authors consider, in addition to the *2f* (*f* is the nominal frequency) current components which rotate in negative sequence, the zero sequence components in the circulating current during the asymmetrical fault condition. Hence, the control signal of negative sequence is augmented with an abc frame signal that contributes to eliminating zero sequence ripples. Authors report that the proposed method shows improved transient response since no filtering action is used to extract zero sequence components. A controller which nullifies second order ripples in the Dc bus voltage and current is presented in [14]. The voltage ripple components originates from the difference between the DC voltage and the accumulation of upper and lower arm voltages which are of zero sequence oscillating at $2f$. The controller is tested when the MMC-HVDC system is operating under a fault which leads to an unbalanced AC grid. The paper also investigated AC power, as a function of time, under the effect of positive sequence grid current.

Work in [15] proposed a nested loop control strategy for an MMC based HVDC system. The first loop is used to control the AC current towards a calculated

positive sequence reference, nullifying at the same time the negative sequence current under an unsymmetrical fault. Control is achieved through a non-ideal proportional +resonant (P+PR) controller implemented in the αβ frame. The second loop of the nest, eliminate the AC fluctuations in the circulating current of the converter arm. Authors derived an analytical expression which shows that circulating current contains positive, negative and zero sequence rotating at double the nominal frequency. The non-ideal P+PR shows a robust response to frequency alterations. Due to the star/delta transformer at both the sending and receiving ends of the HVDC system, the zero sequence voltage or current in output lines is not considered in the analysis. Control is considered for MMC in [16] based on analytical expression for phase power in terms of symmetrical components. Control is based on a two stage strategy. The first stage represents a fast response control loop that regulates sequence currents to reference values. The second stage, with a slow response, generates the reference values for sequence currents. The paper considers two approaches for determining reference settings. The first, calculates the positive sequence components based on the reference active and reactive power settings, whereas the negative sequence current is driven to zero. Second approach is based on obtaining current references by nullifying double line frequency power ripples in each phase. Based on results from both strategies, authors concluded that the latter option is not suitable for an MMC system since the ripples in the DC voltage are not suitably suppressed due to the ripples in the sub-module capacitor voltages. Since an HVDC system may operate without a transformer at either ends, due to economic or space related considerations, authors propose a controller which tracks zero sequence current to a zero reference.

Authors in [17] presented an equivalent circuit based method for calculation of sequence circulating current phasor components. Here, the positive, negative and zero sequence voltage components are first expressed mathematically then the corresponding sequence currents are determined from the equivalent circuit corresponding to each sequence. Two scenarios are explored in the calculation process; first the MMC operates under unbalanced grid conditions where the three phase currents remain unbalanced. The second is a case where the AC currents are forcefully balanced, by driving the negative sequence current to zero. Analytical expressions shows that with the later condition, contribution of ripple voltage, at double the nominal grid frequency, are accumulated from a variety of terms making the determination of sequences current components denser. An all-inclusive approach is suggested in [18] to achieve a number of objectives through controlling the arm current of MMC. Here, the objective includes; balancing the AC line currents, nullifying the circulating current and controlling the zero sequence current in scenarios where a path exists for its flow. Authors base the approach on achieving DC/AC power equivalence. Under unbalanced conditions the DC current, per leg, is no longer equal to 1/3 the total current, but the AC line currents can be equalized and hence power equilibrium is achieved.

Due to the wide list of advantages, an MMC could be utilized in other applications such as interfacing distributed energy sources to utility grids operating as a part of a microgrid. Here, the voltage profiles will exhibits an asymmetrical and/or distorted behavior at the PCC [19]. On the other hand, literature [14-18] mainly investigates control methods and/or modeling of arm currents under an asymmetrical grid voltage conditions. These conditions reflects mainly a fault, normally can be cleared within a specified time, such as one line to ground short circuit in applications within the context of HVDC. The contribution of this paper is to investigate the following points in relation to a DC source interfaced to a PCC through an MMC;

1. Modeling of arm currents with the existence of zero sequence current and voltage at the PCC due to the sustainable unbalanced voltage profile. Hence, no blocking mechanism exists in the path of the zero sequence current.
2. Analyzing the circulating current components implicitly under the unbalanced PCC voltage and current.
3. Evaluating voltage balancing techniques for the considered interfacing application. Since the converter is operated to inject power towards the PCC, the magnitude of the converter output voltage dictates the amount of power flow. Hence voltage balancing technique is critical in this application.

To the best knowledge of the authors, the practice of evaluating capacitor voltage balancing methods under asymmetrical grid conditions, for an interfacing MMC application, is not discussed in present literature. Therefore, this paper will consider two balancing techniques and evaluate their performance under an asymmetrical PCC voltage.

The rest of this paper is organized as follows. Section 2 describes the operation of an MMC and the proposed system. Section 3 presents a mathematical formula for the converter arm current

under an unbalanced PCC conditions, with the existence of zero sequence voltage and current components. Voltage balancing techniques investigated in this work for sub-modules capacitors are outlined in section 4. Simulation and discussion of results are presented in section 5. Finally, the paper ends with conclusion remarks.

2. The modular multilevel converter and proposed system

2.1 Converter operation

The MMC converter is composed from three branches, each one reflecting an AC phase. Each branch is composed from two arms; an upper and a lower arm. The arms hold a number of sub-modules which are comprised from converters that are either half or full bridge configuration. Fig. 1, shows the schematic of the MMC, where Ro and Lo are the arm resistance and inductance respectively. Point O is considered as an imaginary ground [8]. One of the main differences of the MMC, when compared to the other voltage source topologies, is that the capacitors are related to each sub-module rather than positioned at the input DC terminals of the converter [16]. According [3], the output voltage from a sub-module assumes two values; either the capacitor voltage,V_c , when a PWM signal associated with a sub-module is high, or zero when the triggering command is low. Since the two arms per branch have identical number of sub-modules [3], switching status of opposite arms sub-modules operate in a complementary manner. For example, if N_{uon} and N_{loff} are the numbers of ON and OFF sub-modules in the upper and lower arms respectively, then at any instant,

$$N_{uon} = N_{loff} \tag{1}$$

Also, the number of OFF and ON sub-modules in the upper and lower arms, N_{uoff} and N_{lon} are given by,

$$\begin{aligned} N_{uoff} &= N_u - N_{uon} \\ N_{lon} &= N_l - N_{loff} \end{aligned} \tag{2}$$

The output voltage at the AC side of the converter, relative to point O, if $N_u = N_{uon}$ (that is $N_{uoff} = N_{lon} = 0$) is given by,

$$V_{aO} = \frac{V_{Dc}}{2} \tag{3}$$

For each instant that requires an addition (removal) of a lower (upper) sub-module, N_{lon} is increased by 1 (N_{uon} is decreased by 1). Hence, the output voltage in general is expressed by,

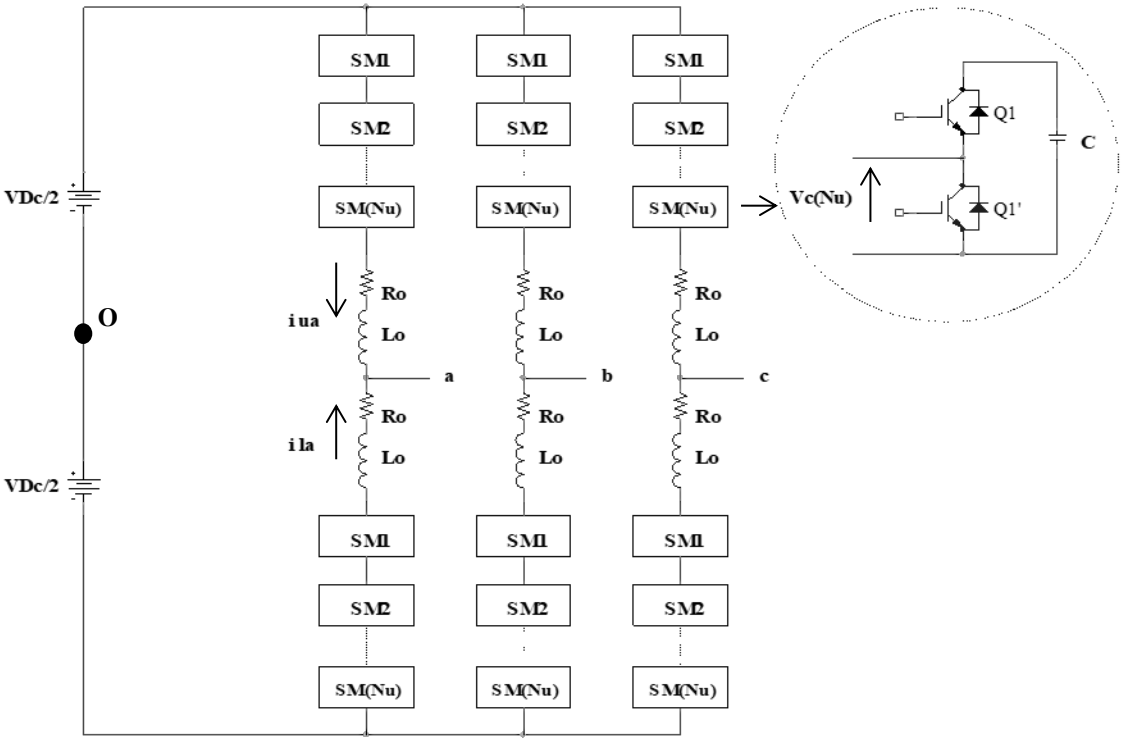


Figure. 1 Modular multi-level converter with a half bridge sub-module

$$V_{aO} = \frac{V_{Dc}}{2} - N_{lon}\frac{V_{Dc}}{N_u} \quad (4)$$

Here, Eq. (4) is based on the ideal case that the capacitor voltages of all incoming sub-modules are equal. Therefore, according to Eq. (4), the voltage levels in the output AC terminals will be in the range of $[\frac{-V_{Dc}}{2}, \frac{V_{Dc}}{2}]$.

2.2 System under study

The aim of this paper is to study a distributed energy source interfaced through an MMC to a utility distribution grid. The system under study is shown in Fig. 2. Here, Rs and Ls are the filter resistance and inductance, per phase, respectively. Compared to a HVDC system, the system considered in this work has,

1. No transformer to block zero sequence current at PCC, hence this current should be accounted for at conditions of unbalanced PCC voltage profile.
2. No high impedance to ground, whereas for HVDC systems such impedance is present [17], hence a zero sequence current path is obstructed. Accordingly, the interfacing MMC system considered in this study has direct connection to ground.
3. The mid-point, O, for the DC terminals is grounded [16] and tied to the neutral side of the utility grid.

At the rated frequency of the grid, arm currents,i_{uy} and i_{ly} (y=a, b, c) can be expressed as the sum of output and internal circulating currents [20], hence,

$$i_{uy} = \frac{i_{pccy}}{2} + i_{cy} \quad (5)$$

$$i_{ly} = -\frac{i_{pccy}}{2} + i_{cy} \quad (6)$$

Directly from Eq. (5) and Eq. (6), the circulating current can be obtained as half the sum of i_{uy} and i_{ly} . This current is generally decomposed into a DC component (i_{cdy}) and a number of frequency components, expressed as a Fourier series [20],

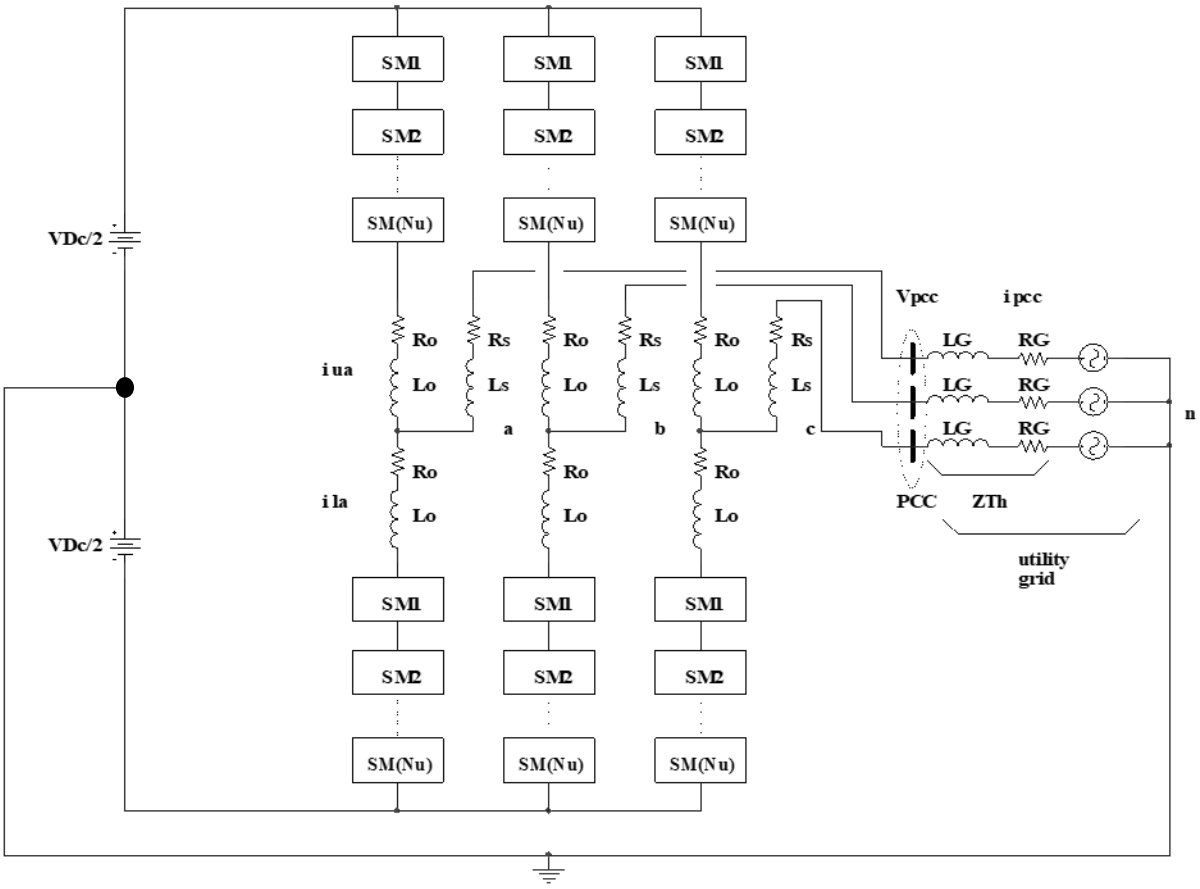


Figure. 2 System under study

$$i_{ca} = i_{cda} + \sum_{n=1}^{\infty} I_{cn} \cos(2\pi nft + \delta_n) \quad (7)$$

Here Eq. (7) expresses circulating current of phase a. A Similar expression for the circulating current of phase b and c can be obtained.

3. Arm currents expressions under unbalanced voltage and current at point of common coupling

Unbalanced PCC voltage and eventually current result from terminal conditions of the utility grid. The phasor magnitude of PCC voltage and current in terms of sequence components can be expressed as,

$$V_{pcc}^{012} = A^{-1} V_{pcc}^{abc} \quad (8)$$

$$I_{pcc}^{012} = A^{-1} I_{pcc}^{abc} \quad (9)$$

Here, the matrix A is the symmetrical components transformation matrix [21] and notation 012 refers to zero, positive and negative sequence components respectively. From the above information, the instantaneous voltage and current quantities at the PCC are expressed as,

$$\begin{aligned} v_{pccy} = {} & V_{pcc}^0 \cos(2\pi ft + \theta_v^0) \\ & + V_{pcc}^1 \cos(2\pi ft + \theta_v^1 \\ & - 2\pi k/3) \\ & + V_{pcc}^2 \cos(2\pi ft + \theta_v^2 \\ & + 2\pi k/3) \end{aligned} \quad (10)$$

$$\begin{aligned} i_{pccy} = {} & I_{pcc}^0 \cos\left(2\pi ft + \theta_i^0\right) \\ & + I_{pcc}^1 \cos\left(2\pi ft + \theta_i^1 \right. \\ & \left. - 2\pi k/3\right) \\ & + I_{pcc}^2 \cos\left(2\pi ft + \theta_i^2 \right. \\ & \left. + 2\pi k/3\right) \end{aligned} \quad (11)$$

The constant k has a value that depends on the phase considered. For phase a, the value of k=0, for phase b, k=1 and k=2 for phase c. The power equilibrium at the input/output ports, per leg (phase), can be written as,

$$P_{iny} = P_{pccy} + P_{lossy} \quad (12)$$

Where P_{iny}, P_{pccy} *and* P_{lossy} are the input power, output AC power and leg losses of phase y respectively. The input leg power is the sum of upper and lower arm effects, hence,

$$\begin{aligned} & 0.5\, V_{Dc} i_{uy} + 0.5\, V_{Dc} i_{ly} \\ & \qquad = v_{pccy}\, i_{pccy} + P_{lossy} \end{aligned} \quad (13)$$

Substituting Eqs. (5) and (6) into Eq. (13) and assuming the MMC system is 100% efficient [15], the input/output power balance is expressed as,

$$V_{Dc}\, i_{cy} = v_{pccy}\, i_{pccy} \quad (14)$$

By substituting Eqs. (10) and (11) into Eq. (14), three terms are obtained. Here, for simplicity, each term is expressed separately as shown in Eq. (15).

$$\begin{aligned} i_{cy1} = {} & \frac{V_{pcc}^0 I_{pcc}^0}{2V_{Dc}} \left[\cos(\theta_v^0 - \theta_i^0) + \cos(4\pi ft + \theta_v^0 + \theta_i^0)\right] \\ & + \frac{V_{pcc}^0 I_{pcc}^1}{2V_{Dc}} \left[\cos(\theta_v^0 - \theta_i^1 + 2\pi k/3) + \cos(4\pi ft + \theta_v^0 + \theta_i^1 - 2\pi k/3)\right] \\ & + \frac{V_{pcc}^0 I_{pcc}^2}{2V_{Dc}} \left[\cos(\theta_v^0 - \theta_i^2 - 2\pi k/3) + \cos(4\pi ft + \theta_v^0 + \theta_i^2 + 2\pi k/3)\right] \end{aligned} \quad (15a)$$

$$\begin{aligned} i_{cy2} = {} & \frac{V_{pcc}^1 I_{pcc}^0}{2V_{Dc}} \left[\cos(\theta_v^1 - \theta_i^0 - 2\pi k/3) + \cos(4\pi ft + \theta_v^1 + \theta_i^0 - 2\pi k/3)\right] \\ & + \frac{V_{pcc}^1 I_{pcc}^1}{2V_{Dc}} \left[\cos(\theta_v^1 - \theta_i^1) + \cos(4\pi ft + \theta_v^1 + \theta_i^1 - 4\pi k/3)\right] \\ & + \frac{V_{pcc}^1 I_{pcc}^2}{2V_{Dc}} \left[\cos(\theta_v^1 - \theta_i^2 - 4\pi k/3) + \cos(4\pi ft + \theta_v^1 + \theta_i^2)\right] \end{aligned} \quad (15b)$$

$$\begin{aligned} i_{cy3} = {} & \frac{V_{pcc}^2 I_{pcc}^0}{2V_{Dc}} \left[\cos(\theta_v^2 - \theta_i^0 + 2\pi k/3) + \cos(4\pi ft + \theta_v^2 + \theta_i^0 + 2\pi k/3)\right] \\ & + \frac{V_{pcc}^2 I_{pcc}^1}{2V_{Dc}} \left[\cos(\theta_v^2 - \theta_i^1 + 4\pi k/3) + \cos(4\pi ft + \theta_v^2 + \theta_i^1)\right] \\ & + \frac{V_{pcc}^2 I_{pcc}^2}{2V_{Dc}} \left[\cos(\theta_v^2 - \theta_i^2) + \cos(4\pi ft + \theta_v^2 + \theta_i^2 + 4\pi k/3)\right] \end{aligned} \quad (15c)$$

The upper arm current (only upper arm is shown due to space limitation) is found by substituting Eq. (15) into Eq. (5). Here for simplicity, the DC component, zero, positive and negative sequence contribution is written separately as in Eq. (16).

$$i_{uy}^{dc} = \frac{V_{pcc}^0 I_{pcc}^0}{2V_{Dc}} \cos(\theta_v^0 - \theta_i^0) + \frac{V_{pcc}^0 I_{pcc}^1}{2V_{Dc}} \cos(\theta_v^0 - \theta_i^1 + 2\pi k/3) + \frac{V_{pcc}^0 I_{pcc}^2}{2V_{Dc}} \cos(\theta_v^0 - \theta_i^2 - 2\pi k/3) + \frac{V_{pcc}^1 I_{pcc}^0}{2V_{Dc}} \cos(\theta_v^1 - \theta_i^0 - 2\pi k/3) + \frac{V_{pcc}^1 I_{pcc}^1}{2V_{Dc}} \cos(\theta_v^1 - \theta_i^1) + \frac{V_{pcc}^1 I_{pcc}^2}{2V_{Dc}} \cos(\theta_v^1 - \theta_i^2 - 4\pi k/3) + \frac{V_{pcc}^2 I_{pcc}^1}{2V_{Dc}} \cos(\theta_v^2 - \theta_i^1) + \frac{V_{pcc}^2 I_{pcc}^2}{2V_{Dc}} \cos(\theta_v^2 - \theta_i^2) \quad (16a)$$

$$i_{uy}^0 = \frac{I_{pcc}^0}{2} \cos(2\pi ft + \theta_i^0) + \frac{V_{pcc}^0 I_{pcc}^0}{2V_{Dc}} \cos(4\pi ft + \theta_v^0 + \theta_i^0) + \frac{V_{pcc}^1 I_{pcc}^2}{2V_{Dc}} \cos(4\pi ft + \theta_v^1 + \theta_i^2) + \frac{V_{pcc}^2 I_{pcc}^1}{2V_{Dc}} \cos(4\pi ft + \theta_v^2 + \theta_i^1) \quad (16b)$$

$$i_{uy}^1 = \frac{I_{pcc}^1}{2} \cos(2\pi ft + \theta_i^1 - 2\pi k/3) + \frac{V_{pcc}^0 I_{pcc}^1}{2V_{Dc}} \cos(4\pi ft + \theta_v^0 + \theta_i^1 - 2\pi k/3) + \frac{V_{pcc}^1 I_{pcc}^0}{2V_{Dc}} \cos(4\pi ft + \theta_v^1 + \theta_i^0 - 2\pi k/3) + \frac{V_{pcc}^2 I_{pcc}^2}{2V_{Dc}} \cos(4\pi ft + \theta_v^2 + \theta_i^2 + 4\pi k/3) \quad (16c)$$

$$i_{uy}^2 = \frac{I_{pcc}^2}{2} \cos(2\pi ft + \theta_i^1 + 2\pi k/3) + \frac{V_{pcc}^0 I_{pcc}^2}{2V_{Dc}} \cos(4\pi ft + \theta_v^0 + \theta_i^2 + 2\pi k/3) + \frac{V_{pcc}^1 I_{pcc}^1}{2V_{Dc}} \cos(4\pi ft + \theta_v^1 + \theta_i^1 - 4\pi k/3) + \frac{V_{pcc}^2 I_{pcc}^0}{2V_{Dc}} \cos(4\pi ft + \theta_v^2 + \theta_i^0 + 2\pi k/3) \quad (16d)$$

Compared to the analytical expression for upper arm current in [15], the DC component of the arm current has four terms associated with either V_{pcc}^0 , I_{pcc}^0 or both. On the other hand, the sequence components in Eq. (16) have only two terms related to either V_{pcc}^0 or I_{pcc}^0 . Therefore, operation and control wise, the contribution of these terms must be considered. As expected these additional components will affect the capacitor voltage ripple. This in turn will affect the problem of balancing the sub-modules capacitor voltage. Since the balancing action is regarded as a crucial part of the MMC operation [2], an evaluation process, which the present work adopts, with the existence of V_{pcc}^0 *and* I_{pcc}^0 provide an insight on the effectiveness of the considered balancing methods. Moreover, the output voltage magnitude, at the fundamental frequency, of the interfacing converter is a decisive factor in determining the power transfer towards the PCC. Features of this voltage are impacted by how well capacitors voltage is balanced [4].

4. Voltage balancing techniques

Capacitor voltage, in an ideal case, should equal to the DC voltage divided by the number of sub-modules in an arm. The main algorithm used for balancing is the basic sorting [8] for which the following requirements should be satisfied;

1. Measurements of sub-module capacitor voltage in upper and lower arms.
2. Arrangement of the above measurements from low to high and high to low.
3. Determination of the number of sub-modules required to be connected/ disconnected depending on the status of the PWM system.
4. Sign detection of upper and lower arm currents.
5. Selection of the sub-modules for connection/ disconnection, constrained according to the sorting lists.

Disadvantages of this method include the excessive switching of devices that increase internal losses with no positive impact on the converter performance [22], not to mention the amount of measured quantities required by the algorithm. However, the capacitor voltages per arm are extensively balanced. The second approach requires much less computation efforts, where balancing is achieved by simply rotating the switching pattern between sub-modules [23-25]. In [24, 25] the rotation is implemented based on the voltage levels in the output AC voltages where gating signals are produced according to the level required. Here patterns change every $f/2$ of a cycle. In this case the capacitors of relevant sub-modules will endure the same switching conditions and eventually reach equilibrium as far as charging and discharging intervals are concerned [24].

In MMC operation that is based on multiple PWM carriers, the exchange of sequence for individual sub-modules is executed by rotating the carriers among the sub-modules pairs [26]. This method is shown in [26] for an MMC with only two sub-modules per arm, where carriers are rotated every quarter of a cycle. In this section, the procedure is extended to an MMC with, $N = N_u + N_l$sub-modules and the MMC is connected to grid with unbalanced voltage. If ω_c is the angular frequency of the carrier system, then the carrier is rotated every,

$$m = \frac{\omega_c}{N} \tag{17}$$

of a cycle.

If we consider an example in which,$N_u = N_l = 4$, then according to Eq. (4), five levels are distinguished. If a pair of sub-modules is defined as, $(1, 3')$, where $1 \in N_u$ and $3' \in N_l$, then this pair is exchanged m times among the N carriers (and their complements). In this case, sub-modules capacitors have approximately identical charging and discharging intervals resulting in a balance of voltage between upper and lower sub-modules.

5. Simulation and results

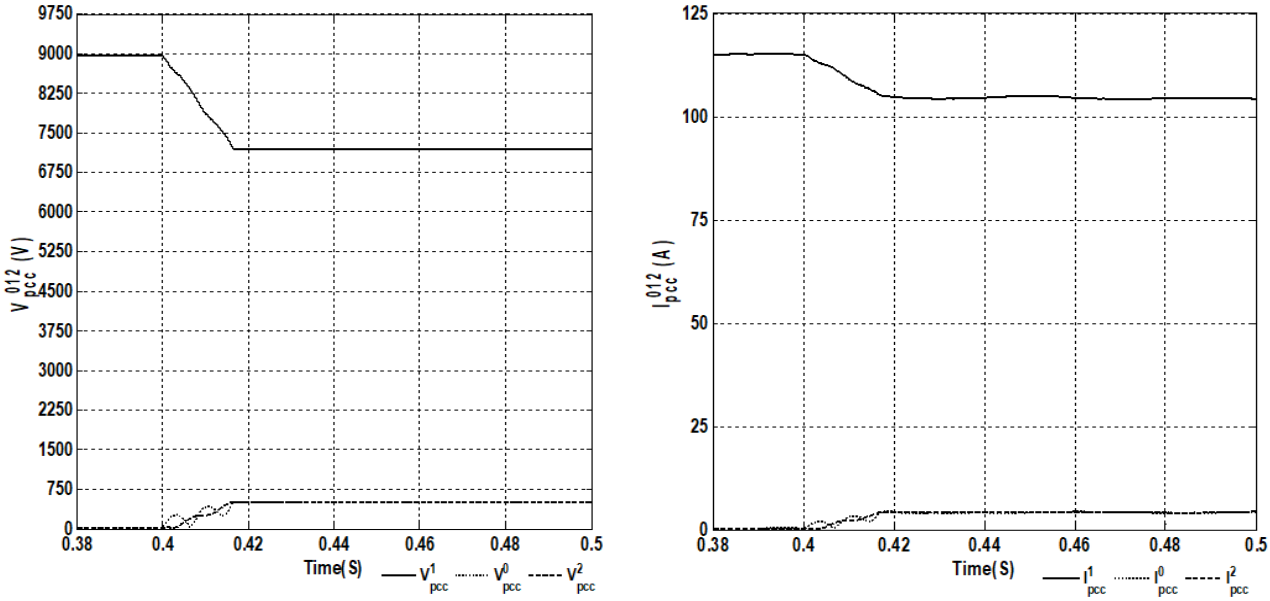
In this section simulation is performed for the system shown in Fig. 2, using Matlab/Simulink platform. The main emphasis is to evaluate the performance of the two balancing techniques; the sorting algorithm and the rotation of PWM carriers. The latter method has been implemented on a two sub-module per arm MMC with a stand-alone RL load in [26]. However, in this paper, a DC energy source is connected to a PCC via an MMC. The PCC has asymmetrical voltage profile. Parameters of the system considered, shown in Table1, are determined based on [26] but modified to the considered system. For both balancing techniques, the converter is modulated by Phase Disposition-PWM (PD-PWM) [8, 27]. In all analysis presented in this work, it is assumed that the utility grid has a high short circuit capacity, hence the Thevenin's impedance is considered to be $Z_{Th} = 1 + j3.77\ m\Omega$ [28].

5.1 Simulation of modular multi-level converter under asymmetrical voltage profile at point of common coupling with carrier rotation based balancing method

In this case an evaluation for the rotation of PWM carriers balancing method is presented. Since the Thevenin's impedance of the grid is low, the voltage profile at the PCC is approximately equal to that of the grid. The grid voltage profile, for each of the respective phases, is scaled down by a factor (less than 1) to simulate the unbalanced conditions. Positive, negative and zero sequence components of voltage and injected current at the PCC are shown in Fig. 3 (a & b) respectively. Hence, an unbalanced voltage and resultant current is present at the PCC. Here, the phase scaling factors are introduced at $t = 0.4\ Sec.$, Fig. 4 depicts the voltage waveforms at the terminals of the MMC converter. It is interesting to note that the output converter voltage is well balanced and the drop in voltage, per phase, is within tolerated limits. In terms of a quantitative description, if phase b of the output voltage is considered, as shown in Fig. 4, at, $0.419 < t \leq 0.424\ Sec$, the peak value is about 9750 V whereas at $0.436 < t \leq 0.443\ Sec$, the peak drops to about 9550 V. Hence the deviation is about 2.04% which represent an acceptable tolerance.

Table 1. System Parameters

Dc energy source voltage, V_{Dc}	19.5 KV
Nominal voltage at PCC, V_G	11 KV (L-L)
Arm resistance per phase, R_{oy}	0 [26]
Arm inductance per phase, L_{oy}	16 mH
Filter resistance per phase, R_{sy}	121 Ω
Filter inductance per phase, L_{sy}	64 mH
Sub-module capacitor, C_{sm}	438 μF
Number of sub-modules per arm, $N_u, (N_l)$	4
AC grid frequency, f	60 HZ
Carrier frequency, F_c	2000 HZ



(a) (b)

Figure. 3 PCC sequence components: (a) voltage and (b) current

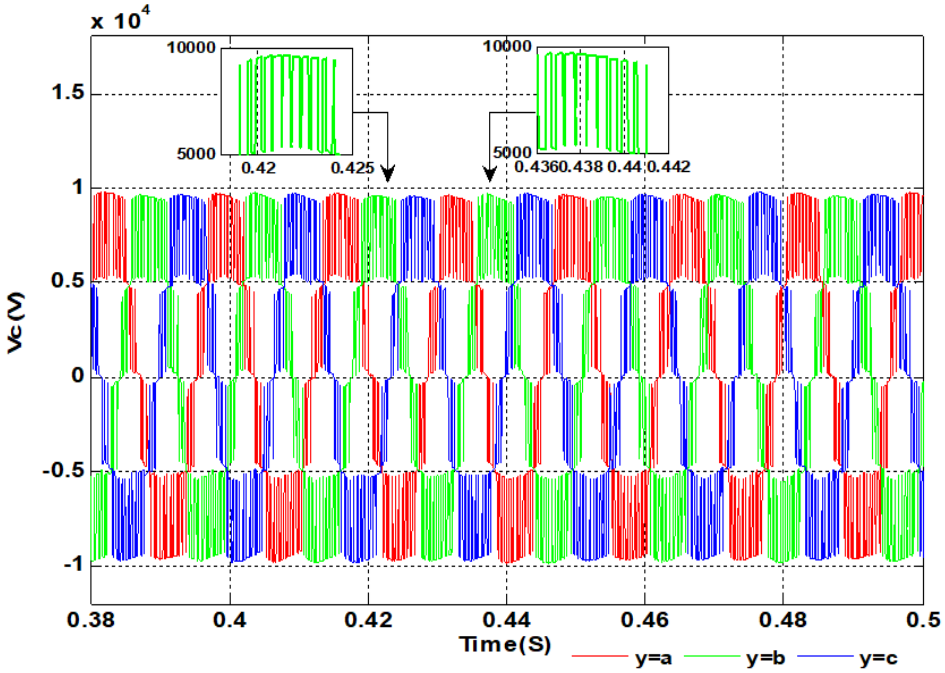


Figure. 4 MMC output voltage

The current at the PCC side is shown in Fig. 5, which shows asymmetrical behavior as expected. PCC currents from the MMC side are seen to have mainly a fundamental component. This complies with the assumption that only fundamental frequency component flow in the AC lines, whereas other components keep circulating within the arm [20]. Hence, the carrier rotation balancing method suffices to fulfill the required quality of current injected to the grid. Upper arm currents, for periods just before and after the initiation of the unbalanced voltage conditions, are shown in Fig. 6. Results show that for $t > 0.4$ Sec the current, per phase, is clamped down due to the DC components contributed by all terms in (16a) except the term, $V^1_{pcc} I^1_{pcc}/2V_{Dc}$, which exists whether the voltage profile is balanced or not, but naturally holds a different value. Hence, the latter term has an effect even before $t = 0.4$ Sec. Therefore, the upper

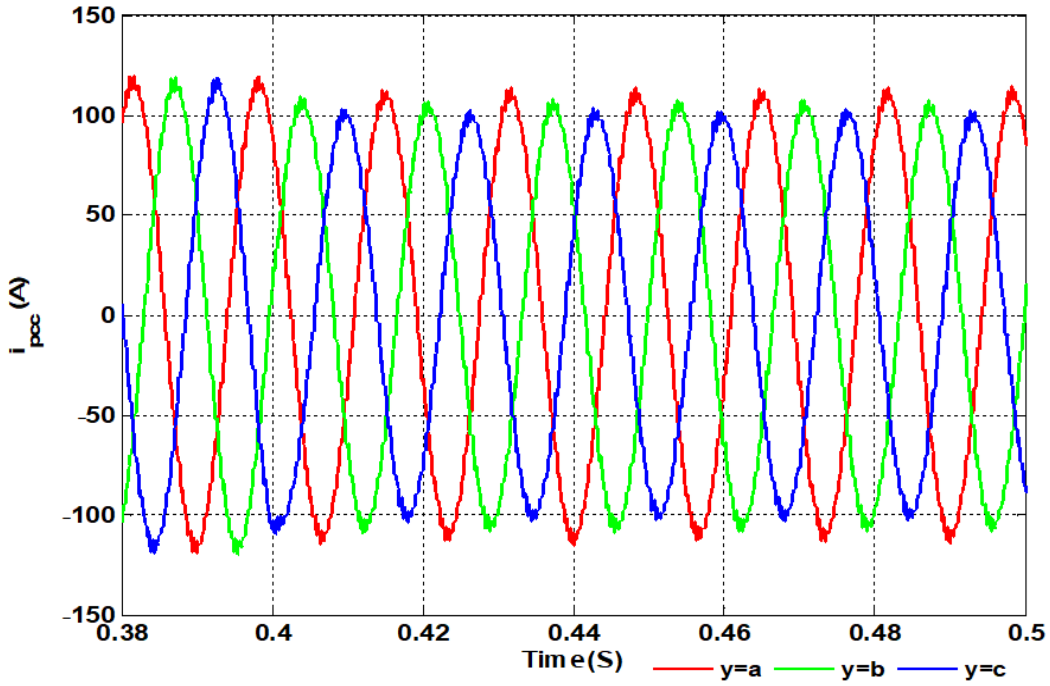


Figure. 5 Current at PCC from converter

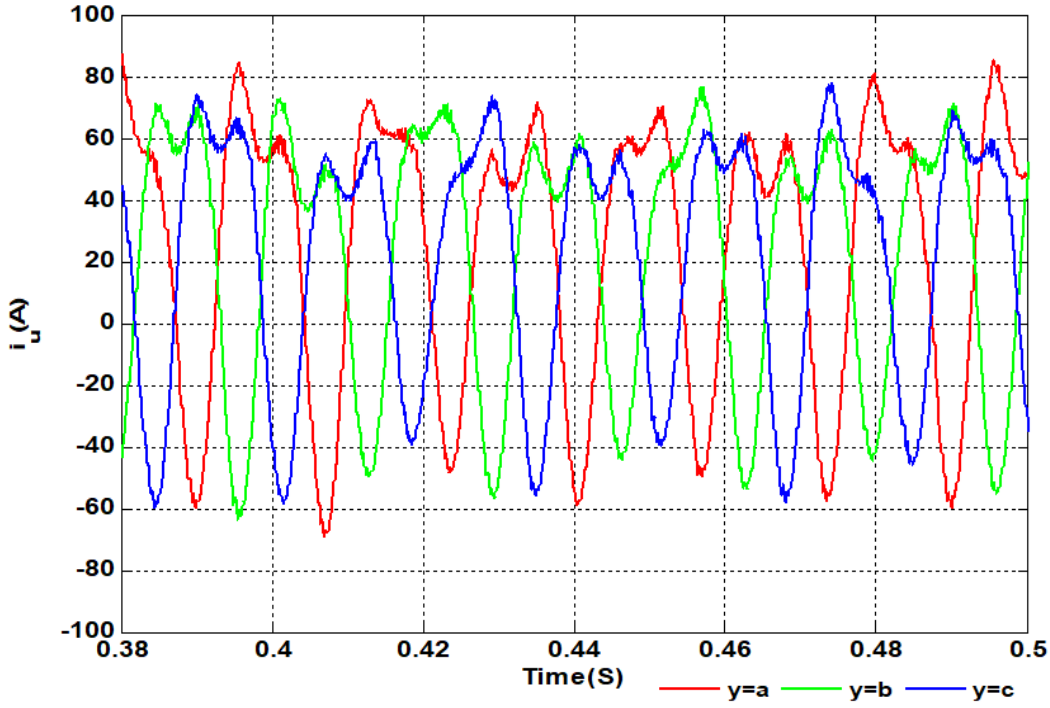


Figure. 6 Upper arm current

arm current for phase y is given by the sum of i_{uy}^{dc}, i_{uy}^{0}, i_{uy}^{1} and i_{uy}^{2}. Finally, the circulating current for y=a, b & c phases are shown in Fig. 7; this current represents components that are circulating within the arm at different frequencies.

5.2 Simulation of modular multi-level converter under asymmetrical point of common coupling voltage profile with sorting based balancing method

In this section, performance of the sorting algorithm is evaluated for the operation of MMC

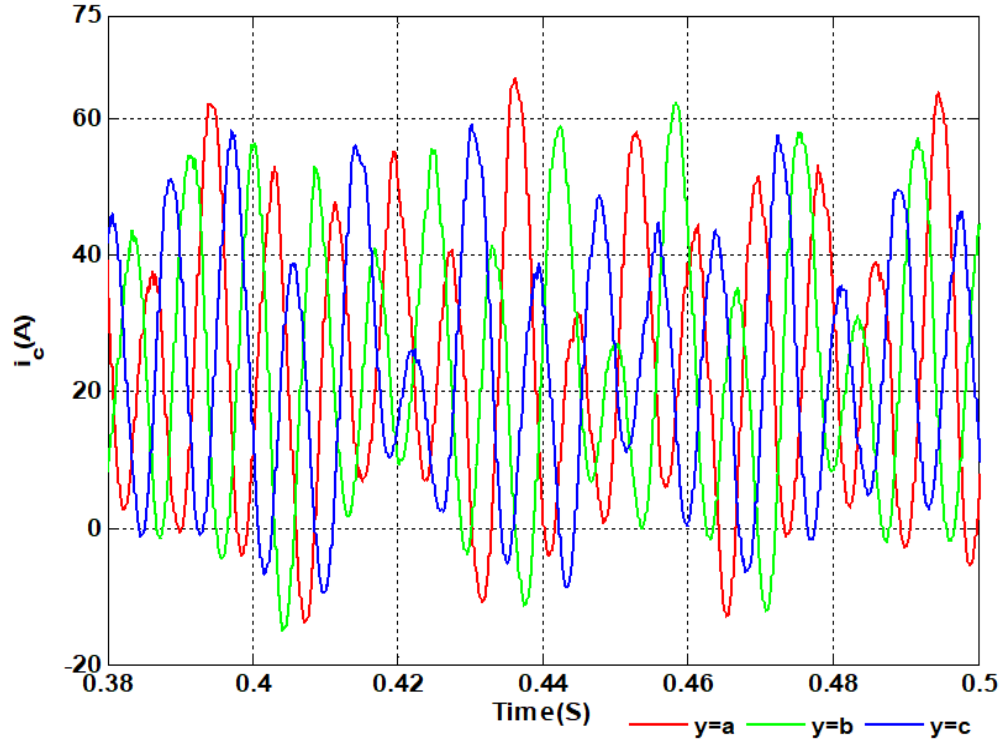


Figure. 7 Circulating current in three legs of converter

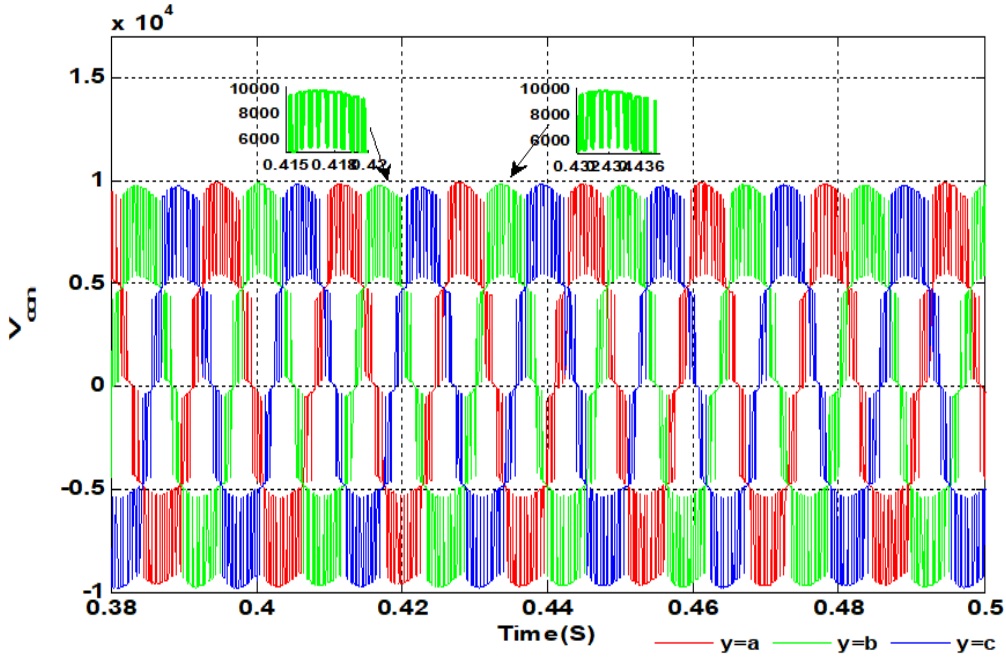


Figure. 8 MMC output voltage for sorting algorithm

under unbalanced PCC voltage condition. In that aspect, the same unbalanced conditions exist at the PCC, hence $V_{pcc}^{012} and\ I_{pcc}^{012}$, have same values as those shown in Fig. 3. Fig. 8 shows the output voltage at the converter terminals, phase b is examined for two consecutive cycles. The first cycle is at a time range of $0.415 \leq t < 0.42\ Sec$ and the second period is at $0.432 \leq t < 0.436\ Sec$, the drop in the voltage is less compared to converter output voltage for the carrier rotation method. However, the difference is in significant considering the drop in the voltage was 2.04% in the rotation method. However, the PCC current, shown in Fig. 9,

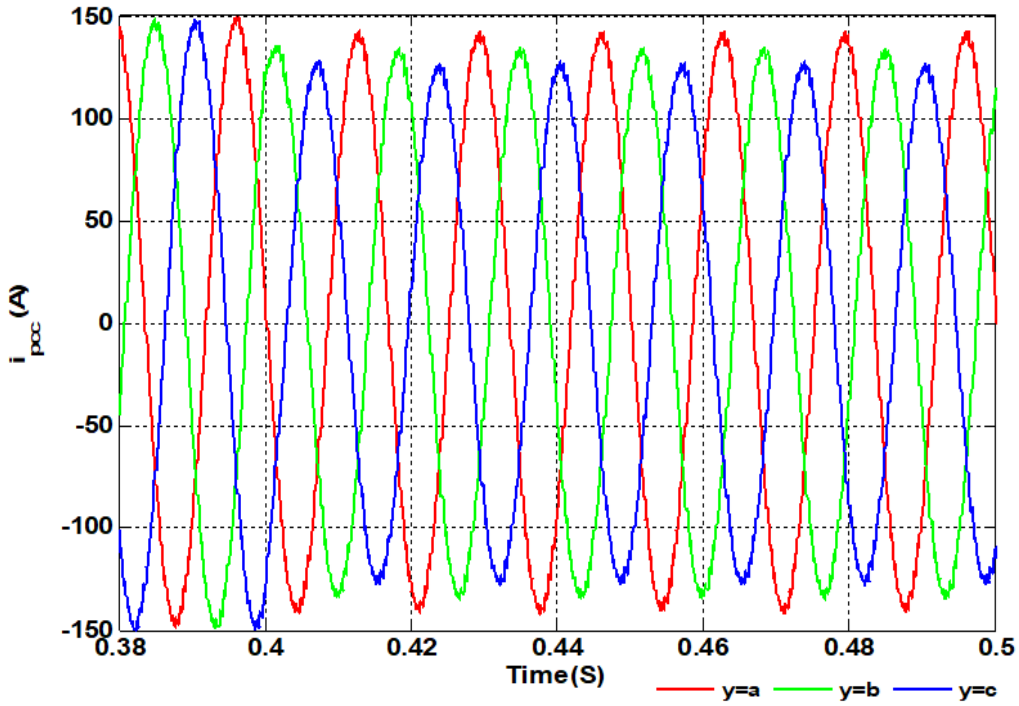


Figure. 9 Current of PCC for sorting algorithm case

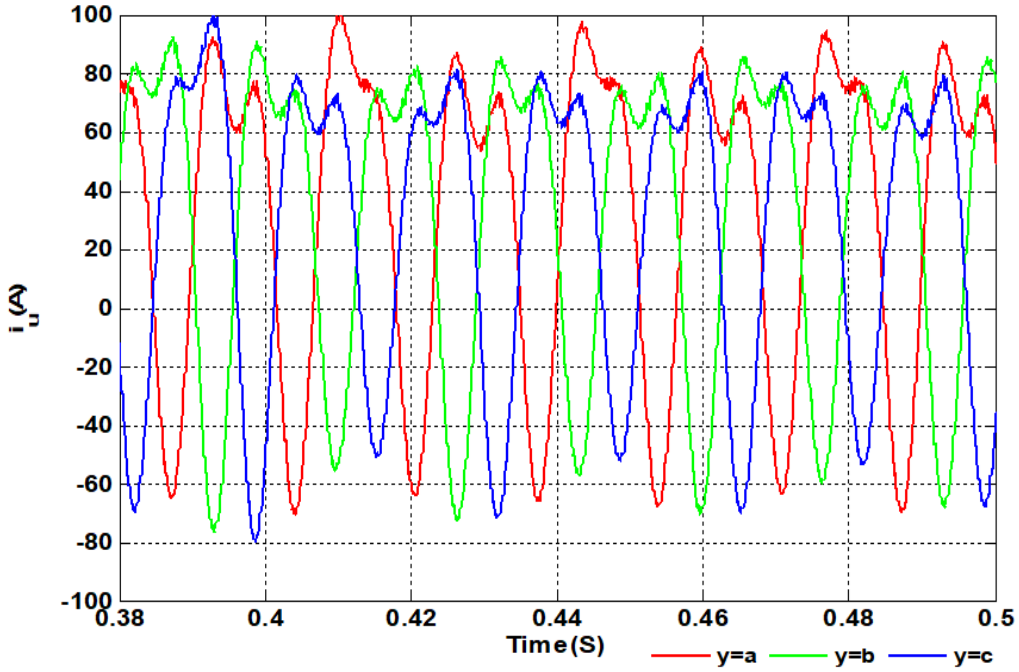


Figure. 10 Upper arm current for sorting algorithm

has a higher magnitude compared to that of the carrier rotation method. This is due to the increased voltage output which results in an increased potential difference, relative to the PCC voltage profile.

If phase A (shown in red on Fig. 9) is examined, for the carrier rotation method, the peak current is 111 A whereas for the sorting algorithm, the peak is about 142 A. One point worth mentioning here is that in both methods, the analysis is carried out at the same modulation index. Hence, the sorting method produces, at the fundamental frequency, a higher voltage compared to the carrier rotation. Upper arm current of the converter is shown in Fig. 10. Here, the current shows an increase compared to that of the rotation method and this is due to the increase in the PCC phase currents. An interesting

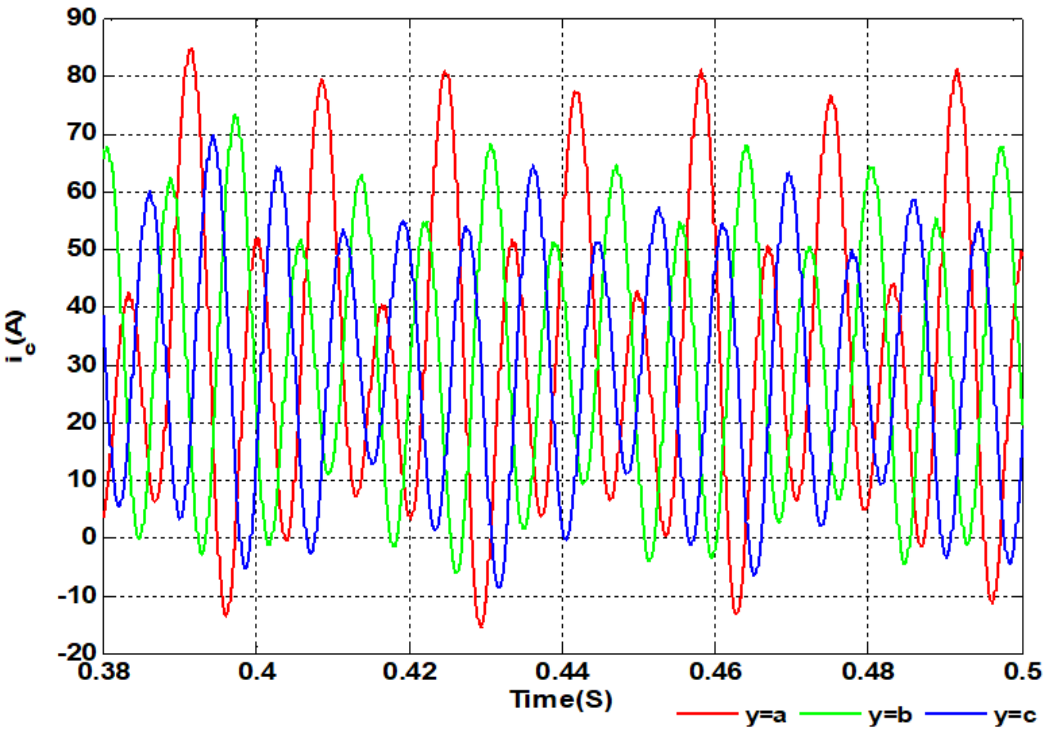


Figure. 11 Circulating current for the sorting algorithm

observation is that the arm current shows less ripple compared to that from the PWM carriers rotation method. This is also reflected in the circulating current of arms shown in Fig. 11. Also, in the sorting method, circulating currents show higher peak values for each arm due to the change in AC line current magnitude. The minor differences between the results obtained from both methods verify feasibility of the carrier rotation method for balancing capacitor voltage in the interfacing MMC under unbalanced grid conditions.

6. Conclusion

In this paper two algorithms, for balancing the capacitor voltage of a sub-module in an MMC, are evaluated under an unbalanced grid connection. The evaluation process is based on the quality of the converter voltage and the injected current to the PCC. The MMC, studied in this paper, is an interfacing converter with a distributed energy source. Unbalanced conditions considered assume a path exist for zero sequence components. Analytical expressions derived reveal that, as a result of zero sequence voltage and current components, additional embedded terms in the arm current are established. The impact of these sequence components are reflected in the mean, zero, positive and negative sequence terms of the arm current. Results verify that the carrier rotation method is feasible to serve as part of the converter modulation process and provide a satisfactory converter operation that supplies AC current with an acceptable ripple content. Although, in the sorting algorithm the voltage harvested at converter terminals is higher, this is evident from the peak value of current injected towards the PCC, yet the voltage deviation in peaks for two consecutive cycles is found to be around 2% in the rotation method. This confirms the feasibility of the rotation method in interfacing applications. Compared to the computation burden of the conventional sorting method, the carrier rotation method can be utilized in control strategies at the MMC level for grid connection applications.

Conflicts of Interest

The authors declare no conflict of interest.

Author Contributions

Conceptualization, Riyadh Toman and Tahani Al-Mhana; methodology, Riyadh Toman and Tahani Al-Mhana, Software, Riyadh Toman; result analysis, Riyadh Toman and Tahani Al-Mhana, writing original draft, Riyadh Toman; review and editing Tahani Al-Mhana.

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