# Design of a High Linearity Four-Quadrant Analog Multiplier in Wideband Frequency Range

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## Abstract

In this paper, a voltage mode four quadrant analog multiplier in the wideband frequency rangeis designed using a wideband operational amplifier (OPAMP) and squaring circuits. The wideband OPAMP is designed using 10 identical NMOS transistorsand operated with supply voltages of ±12V. Two NMOS transistors and two wideband OPAMP are utilized in the design of the proposed squaring circuit. All the NMOS transistors are based on 0.35μm NMOStechnology. The multiplier has input and output voltage ranges of ±10 V, high range of linearity from -10 V to +10 V, and cutoff frequency of about 5 GHz. The proposed multiplier is designed on PSpice in Orcad 16.6.

**Keywords:** Analog multiplier, operational amplifier, squaring circuit, linearity

الخلاصة:

في هذه البحث تم تصميم المضاعف التناظري بنمط الفولتية لنطاق ترددي عريض يعمل في الارباع الاربعة باستخدام المكبرات التشغيلية (OPAMPs) ودوائر التربيع (squaring circuits) ذات المديات العريضة النطاق. ان المكبر التشغيلي المقترح يعمل باستخدام مجهز قدرة ذي فولتيات تجهيز مقدارها12 ± فولت وقد صمم باستخدام 10 ترانزستورات من نوع NMOS. وقد تم استخدام اثنين من الترانزستورات نوع NMOS واثنين من المكبرات التشغيلية ذات النطاق الترددي العريض في تصميم دائرة التربيع المقترحة. جميع الترانسسترات المستخدمة في الدوائر المقترحة تم تصميمها باعتماد تقنية 0.35 مايكرومتر. يمتاز المضاعف التناظري المقترح بمديات ادخال واخراج تصل الى10± فولت وكذلك بعلاقة خطية عالية جدا والتي تمتد من −10 إلى +10 فولت و بتردد قطع يصل الى حوالي 5 غيغاهرتز. تم تصميم المضاعف التناظري واختباره باستخدام برنامج الاوركاد 16.6.

**الكلمات المفتاحية:** المضاعف التناظري ، المكبر التشغيلي، دائرة التربيع ، الخطية

## 1. Introduction

Analog multipliers have been widely exploited in communication circuitries, phase detectors, neural networks, frequency multipliers, mixers, and modulation and demodulation circuits. In conventional applications, such as modulation circuits, the linearity, frequency of operation, and input voltage ranges are issues of great importance for multipliers. In analog signal processing, the need is often revealed for a circuit occupying two analog input signals and generating an output relative to their product. Such circuits are referred to as analog multipliers. If a particular multiplier circuit is designed such that it accepts the polarity of both of its input signals, then the device is designated as a four-quadrant multiplier [Gray and Meyer, 1992].In many communication circuits,analog multipliers are widely utilized in fuzzy logic circuit and neural network applications. In addition, they are widely used in adaptive filters, frequency doubling circuits,phase detectors, function generators, and amplitude modulators [Sharma, 2014]. In the more cases, the functions accomplished by analog multipliers may be carried out with lower costs compared with those using digital signal processing techniques. A digital solution at low frequencies is more effective and cheaper, and permits the circuit function to be adjusted in firmware. When frequencies rise, the cost of realizing digital solutions increases much more than for analog solutions [Misra, 2009].Analog multiplication of signals can be achieved using either a current-mode approach or voltage-mode approach. A voltage-modeapproach stands for abounded linear range. Usually the linear range is expanded at the expense of both circuit complexity and power dissipation. A current-mode approach, furthermore, inherently gives a larger linear range as can be seen from a simple current mirror that shows decades of linearity [Srinivasan, 2006].

In voltage mode multiplier topology, there are many numbers of various architectures proposed for the design of CMOS four-quadrant analog multipliers. Ina work introduced by[Gravati *et.al.*, 2005],fourtranslinear loops with MOS transistors operating in weak inversion were used to form a multiplier,while [Gottiparthy, 2006]had connected MOS transistors at source terminals of input transistors and used them as variable resistors with resistance controlled by bias current. A study conducted by [Kumar,2011] introducedan NMOS four quadrant analog multiplier with supply voltage of 100 mV and -3dB bandwidth of about 60 MHz, while [Liu and Liu,2010]useda multiplier havinga -3dB bandwidth of about 268 kHz with maximum linearity error of about 3.2% corresponding to 120 mV input range.

In order to increase the value of -3 dB bandwidth and improve the frequency response of the arithmetical structures, more analog signal processing functions can be accomplished by taking the squaring characteristic of MOS transistors biased in saturation. CMOS inverters and quarter square technique were utilized for implementing a four quadrant analog multiplier [Machowski *et.al.*, 2008], while [Mokarramand, 2010]had utilized flipped voltage follower and differential squaring circuit for constructing an analog multiplier. A study conducted by[Mallahzadeh *et. al.*, 2010]introduced a multiplier having a cutoff frequency of 5.6 GHz, but low input voltage range of ±100mV.

In a multiplier presented by[Thakare and Tembhurne, 2012], the bandwidth of operation could be adjusted to the ISM band for an input voltage of 0.5 V. There are many different CMOS technologies that could beused in the design of analog multipliers.For example,[Patel and Amin,2014]had used 350 nm and 180 nm CMOS technologiesfor implementinga multiplier consisted of two identical voltage controlled square root blocks and apair of common source amplifiers withinput voltage range of ±1 V.[Soltany and Rezai,2016] introduced a multiplier operated with a very low supply voltage of about 0.15 V and designed with equal sizes of CMOS transistors implemented in 0.18 μm standard CMOS technology.The input voltage ranges of the proposed multiplier were about ±40 mV.

This paper introducesa new voltage mode four-quadrant analog multiplier characterized by high input voltage ranges, high output voltage range, high linearity, and wideband frequency of operation.

**2. The proposed four-quadrant analog multiplier**

The proposed multiplier is based on squaring the sum and difference of the input signals by using two squaring circuits and processing the resulted signals through difference aamplifier as shown in Figure.1.
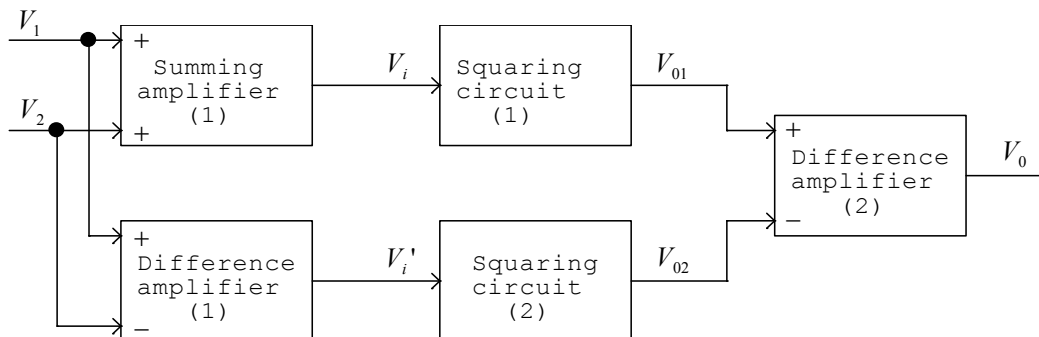


**Figure 1.The block diagram of the proposed squaring circuit and OPAMP based four-quadrant analog multiplier.**

The output voltages$V_i$ of the summing amplifier and $V_i'$ of the first difference amplifier can be given by

$$V_i = A_1(V_1 + V_2) \tag{1}$$
$$V_i' = A_1(V_1 - V_2) \tag{2}$$

Where, $A_1$ represents the voltage gain of both summing and first difference amplifiers. The output voltages $V_{01}$ of the first squaring circuit and $V_{02}$ of the second squaring circuit can be expressed by

$$V_{01} = K_0 + K_1(V_i)^2 \tag{3}$$
$$V_{02} = K_0 + K_1(V_i')^2 \tag{4}$$

Where, $K_0$ and $K_1$ are constants determined by the parameters of the proposed squaring circuit.

Substituting Equations (1) and (2) into (3) and (4), respectively gives

$$\begin{aligned} V_{01} &= K_0 + K_1A_1(V_1 + V_2)^2 \\ &= K_0 + K_1A_1(V_1^2 + 2V_1V_2 + V_2^2) \end{aligned} \tag{5}$$

$$\begin{aligned} V_{02} &= K_0 + K_1A_1(V_1 - V_2)^2 \\ &= K_0 + K_1A_1(V_1^2 - 2V_1V_2 + V_2^2) \end{aligned} \tag{6}$$

The output voltage $V_0$ of the second difference amplifier is

$$V_0 = A_2(V_{01} - V_{02}) = 4A_1A_2K_1V_1V_2 \tag{7}$$

Where, $A_2$ represents the voltage gain of the second difference amplifier. To make $V_1$, $V_2$, and $V_0$ vary in the ranges of $\pm 10V$, the term $4A_1A_2K_1$ can be equated to

$$4A_1A_2K_1 = 0.1 \tag{8}$$

Thus, Equation (7) can be reduced to

$$V_0 = 0.1V_1V_2 \tag{9}$$

## 2.1 Design and analysis of squaring circuit

The squaring circuit is the main and important part in the design of multiplier circuit. It can be carried out by using two n-channel MOSFET (NMOS) connected as shown in Figure 2.In this figure, -*VDD*, +*VDD*, $I_{d1}$, $I_{d2}$, $V_i$, $V_{01}$, $R_{L1}$, and $R_{L2}$ are the negative DC supply voltage, positive DC supply voltage, drain current of the first NMOS transistor (M1), drain current of the second transistor (M2), input voltage, output voltage, drain or load resistance of (M1), and drain or load resistance of (M2), respectively.
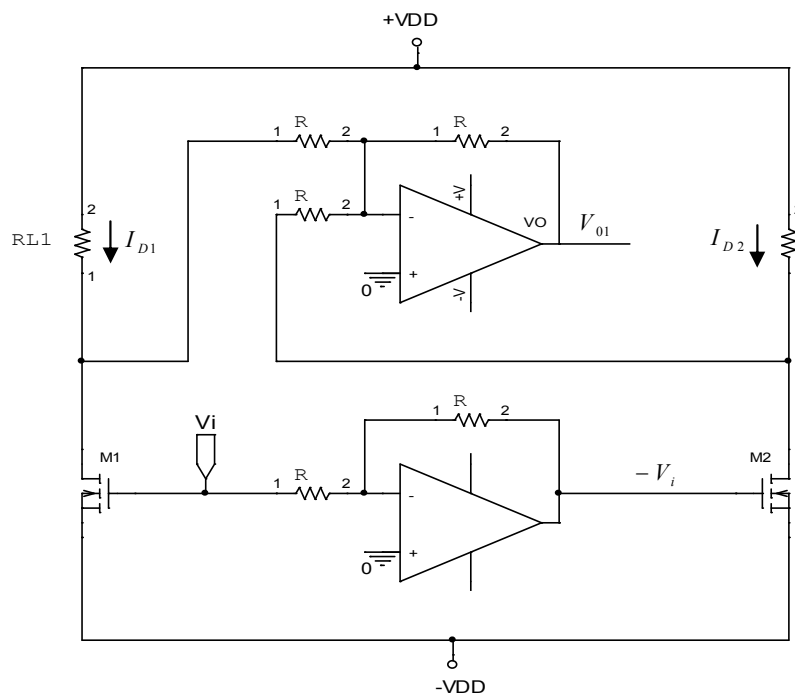


**Figure 2.The proposed squaring circuit.**

The squaring circuit is designed such that $R_{L1} = R_{L2} = R_L$ and both NMOS are designed with the same geometry and their output current $I_{d1}$ and $I_{d2}$ can be given by (Binkley, 2008)

$$I_{d1} = \frac{1}{2} K_P \frac{W}{L} (V_{gs1} - V_{tn})^2 \quad V_{DS} > V_{DSsat} \tag{10}$$

$$I_{d2} = \frac{1}{2} K_P \frac{W}{L} (V_{gs2} - V_{tn})^2 \quad V_{DS} > V_{DSsat} \tag{11}$$

Where $L$ is NMOS effective channel length, $W$ is effective channel width, $V_{gs1}$ is the first NMOS gate to source voltage, $V_{gs2}$ is the gate to source voltage of the second NMOS, $V_{tn}$ is the NMOS threshold voltage, $V_{DS}$ is the drain to source voltage, $V_{DSsat}$ is the saturated drain to source voltage, and $K_P$ is a process parameter defined by [Kang and Leblebigi, 2003].

The output voltage ($V_{01}$) of squaring circuit can be given by

$$V_{01} = -(V_{DD} - I_{d1} R_L + (V_{DD} - I_{d2} R_L)) \tag{12}$$

Substituting Equations (3) and (4) into (5) gives

$$V_{01} = - \left( 2V_{DD} - \frac{1}{2} K_P \frac{W}{L} R_L \left( (V_{gs1} - V_{tn})^2 + (V_{gs2} - V_{tn})^2 \right) \right) \tag{13}$$

But, $V_{gs1}$ and $V_{gs2}$ can be determined by

$$V_{gs1} = V_{DD} + V_i \tag{14}$$

$$V_{gs2} = V_{DD} - V_i \tag{15}$$

Substituting Equations (14) and (15) into (13) results in

$$V_{01} = K_P \frac{W}{L} R_L (V_{DD} - V_{tn})^2 - 2V_{DD} - K_P \frac{W}{L} R_L V_i^2 \tag{16}$$

Comparing Equations (3) and (4) with (16) yields

$$K_0 = K_P \frac{W}{L} R_L (V_{DD} - V_{tn})^2 - 2V_{DD} \tag{17}$$

$$K_1 = -K_P \frac{W}{L} R_L \tag{18}$$

## 2.2 The proposed wideband OPAM

The proposed wideband OPAMP is designed using 0.35 µm NMOS technology with identical NMOS transistors having an effective channel length of 0.35 µm and width of 5.8 µm. The circuit is designed with a positive DC power supply of +12V and negative power supply of -12V. Figure 3 shows the circuit diagram of this OPAMP.
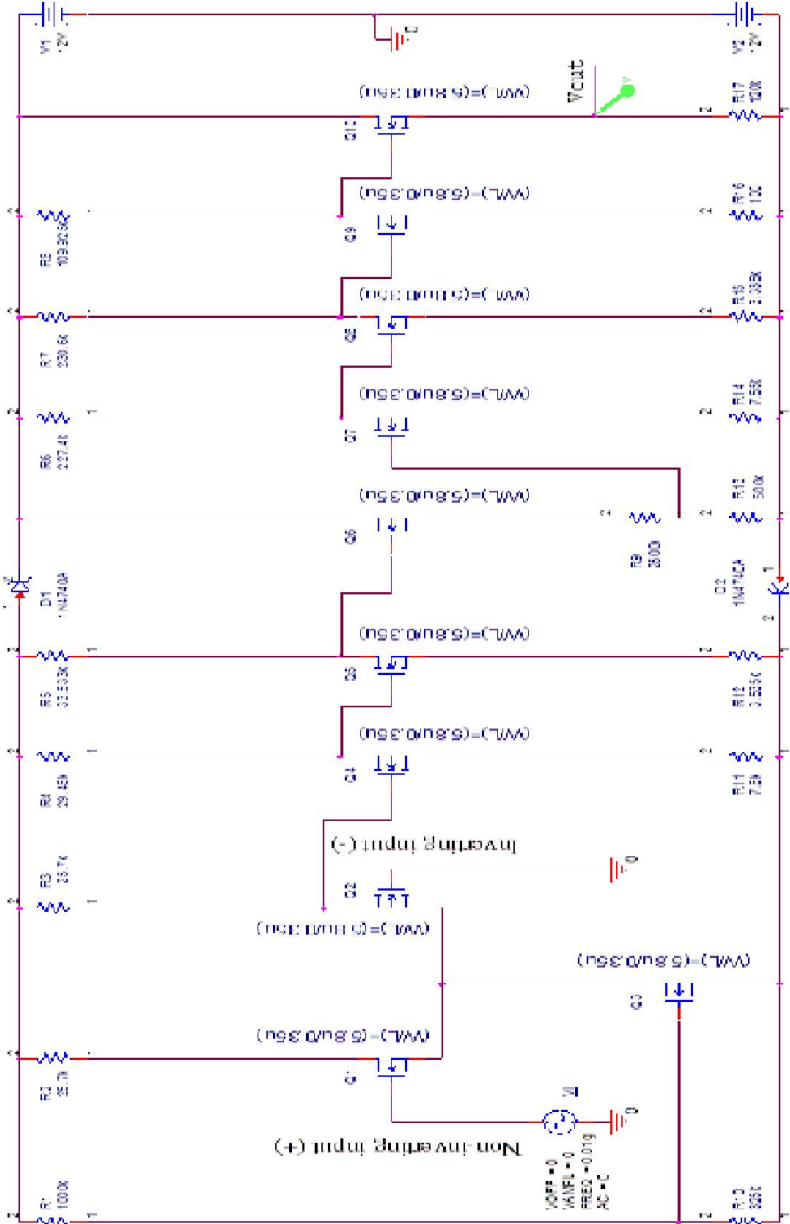.

Figure 3.The Proposed Wideband OPAMP Using (W/L)=(5.8 u/0.35 u) NMOS

## 2.3 The complete multiplier

The complete circuit design of the four-quadrant analog multiplier using OPAMP and squaring circuits is shown in Figure 4.It is designed according to the block diagram shown in Figure 1. It containstwo difference amplifiers,one summing amplifier,and two squaring circuits. In this design, the supply voltages of the squaring circuits are +1 V for $+V_{DD}$ and -1 V for $-V_{DD}$.
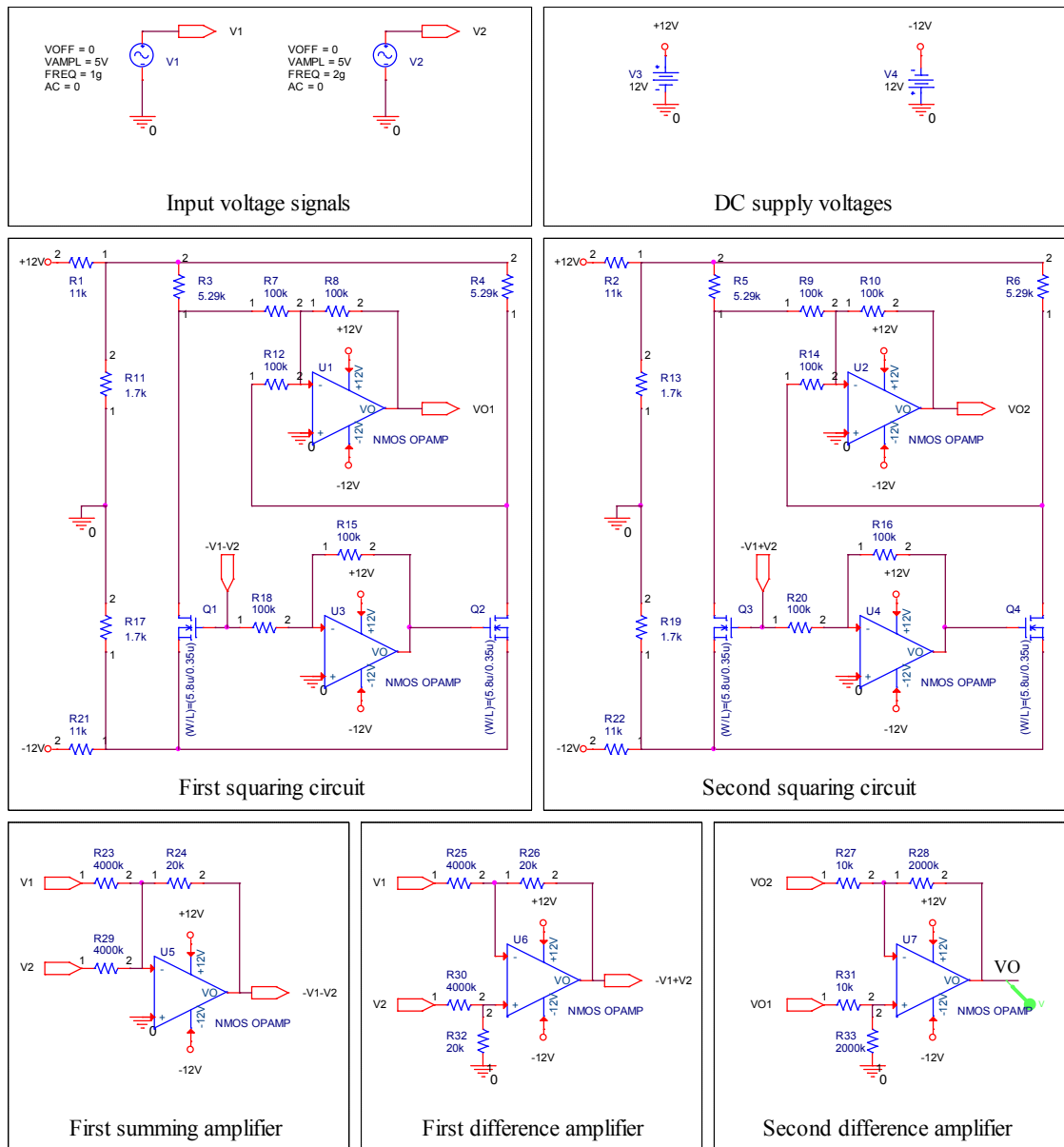
**Figure 4.The circuit diagram of the proposed wideband four-quadrant multiplier using OPAMP and squaring circuits.**

## 3. Results and discussion

The test of the DC input-output characteristics of the proposed OPAMP is shown in Figure 5. In this figure, the non-inverting input of the OPAMP $V_{in}$ is varied linearly between -20 µV and +20 µV. This test shows that the OPAMP output voltage approaches its positive saturation value (slightly greater than +10 V) at $V_{in}$ of 5 µV and negative saturation value (slightly less than -10 V) at $V_{in}$ of -5 µV. It is obvious that this test shows extremely high sensitivity offered by the proposed OPAMP to very small input changes.
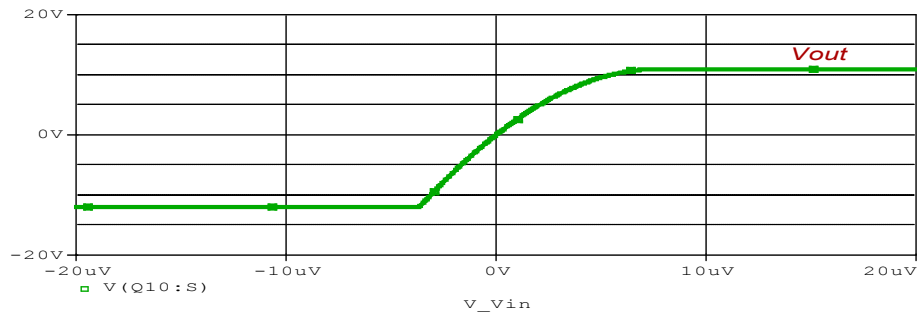
**Figure 5. The input-output DC test during linear change of the non-inverting input of the proposed OPAMP between -20μV and +20μV.**

The frequency response of the proposed OPAMP is revealed through AC sweep test shown in Figure 6. The figure represents the output voltage during exciting the OPAMP by an AC input voltage signal of a constantamplitude of 1 µV and frequency sweep of (1MHz to 10 GHz). This test shows a mid-band output voltage of 3.2 V and an upper -3dB frequency $f_C$ of about 0.6 GHz. It is obvious that the mid-band gain (or open loop gain) of this OPAMP is 3.2V/1µV=3.2×10$^6$.In addition, Figure 6shows that the open loop voltage gain exhibits values greater 100000 in the frequency range from 0.6 GHz to slightly less than 10 GHz.
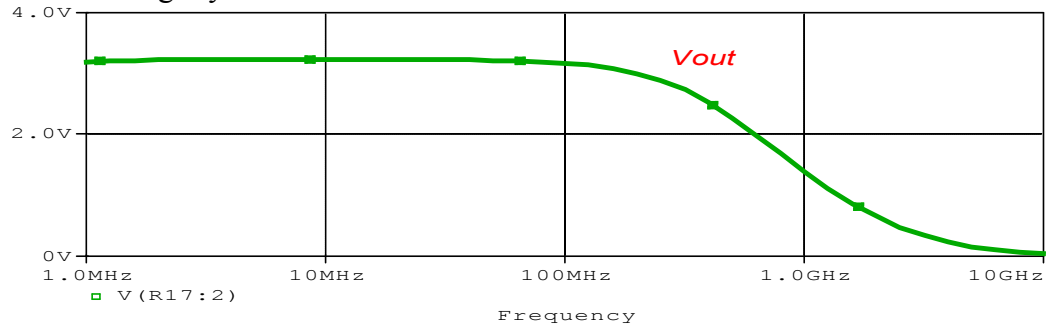


**Figure 6.The frequency response of the proposed OPAMP due to an input voltage of an amplitude of 1 µV and a frequency sweep of (1 MHz to 10 GHz).**

Many tests were proceeded to check the performance of the proposed multiplier described in Figure 4. One of the important properties investigated in this section, is the multiplier linearity in its four quadrants of operation. A second property required to be investigated is the frequency response, which includes bandwidth and frequency range of operation. In addition, this section includes some interesting applications of certain input excitations to reflect the perfect performance of this wideband four-quadrant analog multiplier.To check the linearity of the proposed multiplier in its four quadrants, its first input $V_1$was replaced by a DC voltage sweep of (-10 to +10) V with a step of 0.01 V and its second input $V_2$ was replaced by a parametric DC sweep of (-10 to +10) V with a step of 5 V. The response of this test is shown in Figure 7.
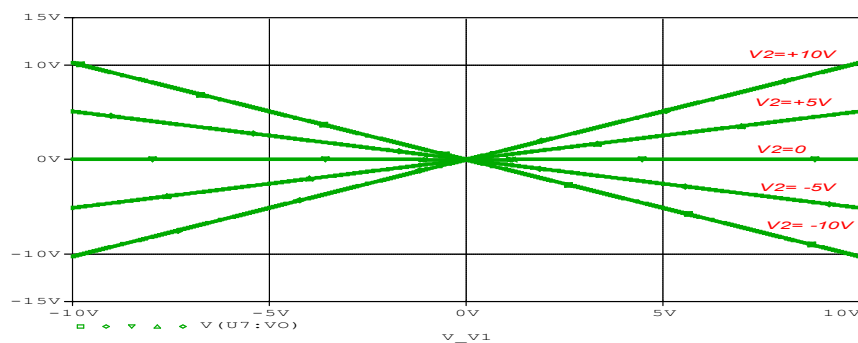


**Figure 7.A linearity test shows the output voltage versus the first input $V_1$ of the proposed multiplier.**

The above test was repeated with the DC voltage sweep on $V_2$ and the parametric DC sweep on $V_1$ as shown in Figure 8. Both Figure 7 and Figure 8 verify that the proposed multiplier is perfectly linear in its four-quadrants and accomplishing very high linearity range of -10 V to +10 V.
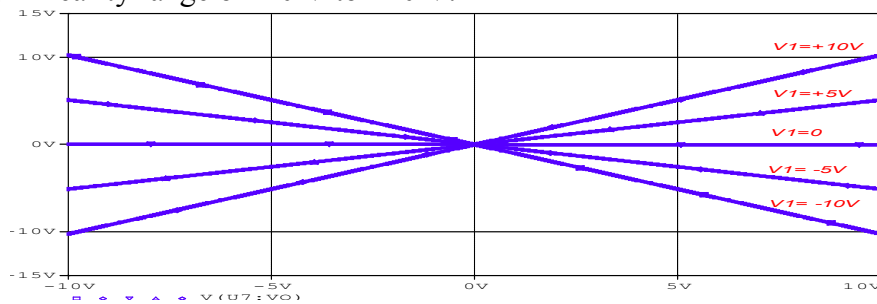


**Figure 8. A linearity test shows the output voltage versus the second input $V_2$ of the proposed multiplier.**

The multiplier frequency range of operation or simply its bandwidth can be measured by applying an AC voltage sweep at one of its input and the other input is excited by a pure DC voltage. Figure 9 shows the frequency response of the proposed multiplier. In this test $V_2$ is excited by a DC voltage of 10 V and $V_1$ is excited by an AC voltage sweep of frequency range of (1 MHz to 5 GHz) with 10 steps per decade. The response reveals a -3dB frequency of about 5 GHz. This is due to high gain OPAMP.
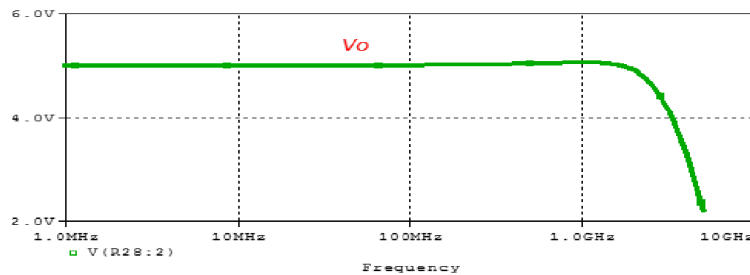


**Figure 9. The frequency response of the proposed multiplier.**

The proposed multiplier can be used as a double sideband amplitude modulator by applying the carrier signal at one of its input and the modulating signal at the other one. Figure 10 represents a test accomplishing this function. In this figure, the carrier signal is a sinusoidal voltage of a frequency of 5 GHz and amplitude of 10 V.
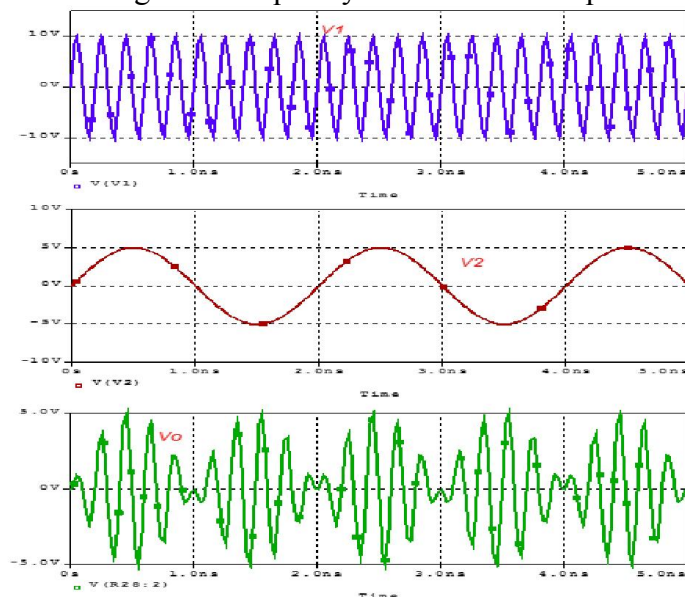


**Figure 10. The proposed multiplier as a double sideband modulator.**

One important function that could be accomplished by this multiplier is a phase modulation test shown in Figure 11. In this test one of the multiplier inputs, is a square voltage waveform (modulating signal) of a frequency of 200 MHz and having voltage levels of ±5 V, while the other input is a 5 GHz sinusoidal signal (carrier) having an amplitude of 10 V. In this test, the phase of the output signal voltage changes by $180^0$ every positive and negative going edges.
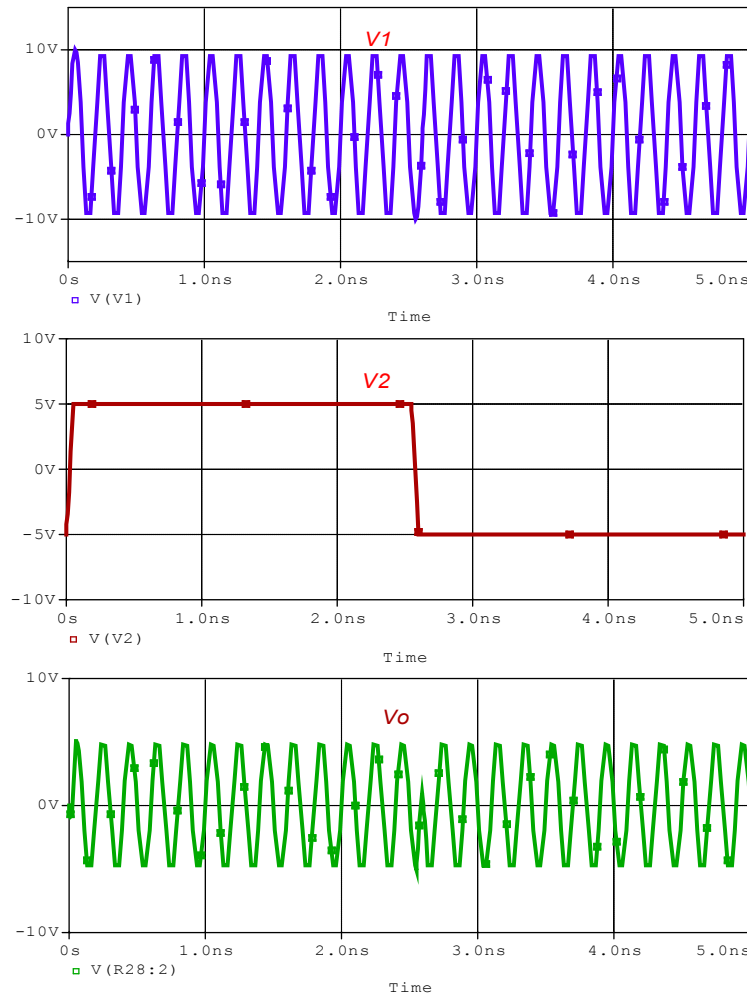


**Figure 11.The proposed multiplier as a phase modulator.**

It is possible to improve the performance of the proposed multiplier by modifying the characteristics of the electronic devices exploited in its design. In addition, with the same electronic devices used in this work, it's possible to design multipliers operating at higher frequencies, but with limited bandwidth. The proposed multiplier, which is designed using NMOS devices built in 0.35 μm technology, shows a cutoff frequency of about 5 GHz, which is greater than that described by [Ghanavati *et.al.,* 2007], which had a cutoff frequency of 1.74 GHz, but with much less input and output voltage ranges or swings. The proposed multiplier has input-output linearity ranges of (-10 V to +10 V), while most of the recent works are operating with very less input-output linearity ranges. For example, the supply voltage of the multiplier suggested by [Sohrabi *et.al.,* 2013] was 1.2 V, whereas the supply voltage of the multiplier introduced by [Soltany and Rezai, 2010] was 0.15 V with input voltage ranges of ±0.04V.

In general, it is much easier to design a multiplier without the voltage ranges and supply voltage constraints than to design it with input and output voltage ranges of ±10 V.

## 4. Conclusions

This work includes the design of wideband squaring and OPAMP circuits exploited in the design of a wideband four-quadrant analog multiplier. The electronic circuits are designed using NMOS transistors processed in 0.35 μm technology. The work is accomplished on PSpice using breakout electronic devices, which are characterized by high transition frequencies. The characteristics of these devices are mainly extracted from their geometries, process technologies, and the physical properties of the semiconductors exploited in their designs. The performance results of the proposed multiplier and the related conclusions are summarized in the followings:

- The wide OPAMP has a very high open loop voltage gain of $3.2 \times 10^6$ and a cutoff frequency of 0.6 GHz. In addition, its open loop voltage gain exhibits values greater than 100000 in the frequency range from 0.6 GHz to slightly less than 10 GHz, thus it makes it possible to exploit this OPAMP in feedback applications throughout this extended frequency range.

- The multiplier has perfect input-output linearity ranges of -10 V to +10 V, which are very much greater than most of those in previous works. It exhibited a cutoff frequency of about 5 GHz, which makes it capable of handling the multiplication of two input signals having a frequency sum in the range of (0 to 5 GHz).

- The multiplier has input and output voltage ranges of ±10 V, which are very much greater than most of those multipliers described in previous works

- Overall, the proposed multiplier with its complementary properties is excellent compared to all multipliers reviewed in this work.

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