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Design of a Linear Synchronous Reactor using a DC Voltage Controlled Statcom

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Abstract

In this paper, a single-phase linearly and continuously controlled synchronous reactor is presented. It is a harmonic-free single-phase statcom. The statcom is constructed of a full bridge voltage source inverter shunted by a DC capacitor and absorbs reactive power from the AC supply through a somewhat small series reactor. The statcom current is controlled linearly by its DC capacitor voltage. The controlling process is achieved by forcing the capacitor to discharge through a boosted up energy tank when its voltage is exceeding the required value and forcing the tank to recharge the capacitor when the capacitor voltage starts to decline. The DC capacitor voltage control in this paper is carried out without needing to external voltage sources. The compensator design is validated on PSpice.

Keywords: Controlled Reactor, Reactive Power, Statcom, Static Var Compensator

1. Introduction

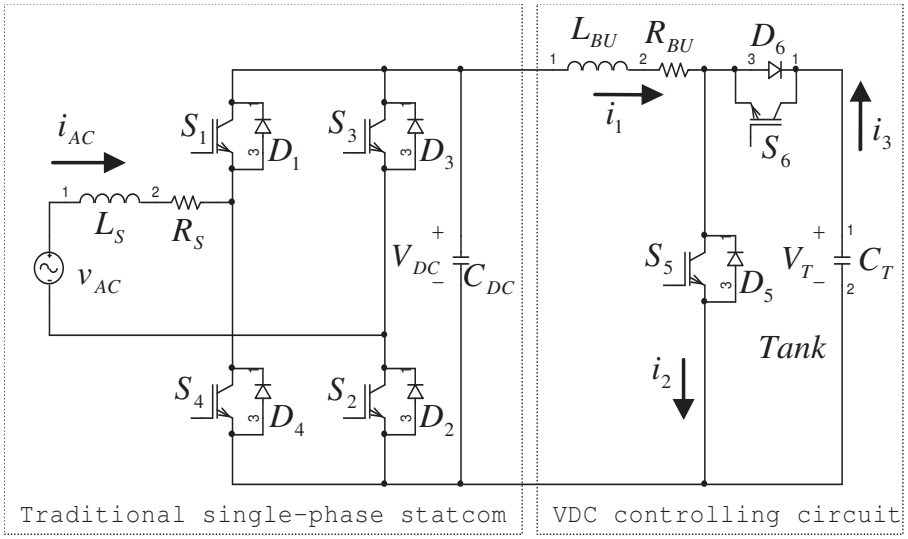
Static Var compensators are the most potent tools employed in field of power quality improvement. They can be used for load balancing of transmission lines, bus-bar voltage control, power factor correction, harmonics elimination, and governing power systems parameters [1-5]. In this paper, only static Var compensators that can be utilized as continuously controlled reactive power absorbers are considered. The thyristor controlled-reactor (TCR) is one of such absorbers, but it releases a wide spectrum of odd current harmonics that increase the transmission losses, disturb the power system network voltage profile, and affect telecommunication systems [6]. A TCR usually requires installation of a harmonic filtering circuitry at it location [7]. Modern static Var compensators are dependent on power conversion techniques and are usually denoted by many designations such as statcoms [8-14]. A three-phase statcom is either a voltage source inverter (VSI) shunted by a DC capacitor and exchanges active and reactive power with the AC supply by small inductors [8-12] or a current source inverter (CSI) shunted by a DC inductor and exchanges active and reactive power with the AC supply by small inductors [13]. A statcom is usually governed by angle control, thus the inverter output voltage is not in phase with the supply input voltage [8, 9]. Generally, the phase currents of power converter-based static Var compensators are not pure reactive and usually contain current harmonics running at the supply frequency multiples and the pulse with modulation carrier frequency multiples [12, 14]. Many techniques were employed to minimize harmonics such as harmonics filtering and utilization of

multilevel technologies in power converters design [9-11]. In this paper, a single-phase statcom-based synchronous reactor is presented. The reactor current is controlled linearly and continuously by the statcom DC capacitor voltage which can be kept at constant profile within its adjusted value. This besides somewhat small series suppressing reactor eliminate all the probable ripples in the current envelope of the proposed synchronous reactor.

2. The Proposed Synchronous Reactor

The proposed synchronous reactor is shown in Figure 1. It is a traditional single-phase statcom equipped with a controlling technique for adjusting its capacitor voltage. The statcom is built of a full-bridge voltage source inverter (FB-VSI) shunted by a DC capacitor C_{DC} and absorbs pure reactive power from the AC supply v_{AC} through a somewhat small harmonic suppressing reactor L_S. Note that R_S is the self-resistance of L_S. The statcom DC voltage controlling circuit is built of a boost up DC-DC chopper and a DC recharging technique. The boost up chopper is formed by L_{BU}, R_{BU}, S_5, D_6, and the energy tank C_T, whereas the recharging process is controlled by the switch S_6.

Figure 1: The proposed synchronous reactor.



The FB-VSI is triggered by the sinusoidal pulse width modulation technique shown in Figure 2. v_{MOD} is the modulating signal which is an analogue sinusoidal voltage in phase with v_{AC} and running with it at the same frequency f. v_{TR} is the carrier signal which is a triangular voltage of frequency f_C. The instantaneous output voltage of the inverter according to this type of triggering can be given by

$$v_{inv} = \frac{V_{DC}}{5}\left(V_{S1} - V_{S3}\right) \tag{1}$$

Assuming that f_C is very much greater than f, the voltage component of v_{inv} at the AC supply fundamental frequency can be given by

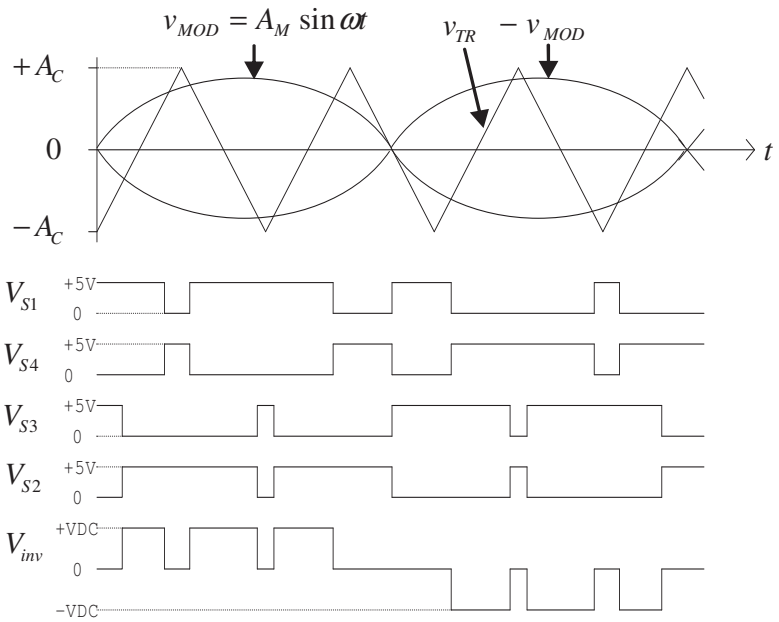
$$v_1 = mV_{DC}\sin\omega t \tag{2}$$

Where, m is the inverter modulation index and is defined as the ratio of v_{MOD} to v_{TR} amplitudes (A_M/A_C). If V_{DC} is kept constant within its adjusted value V_{DCR} and the reactor L_S is chosen such that it can suppress all the harmonic current components running at the multiples of f_C, then the compensator current i_{AC} will be given by

$$i_{AC} = \frac{\left(V_m - mV_{DCR}\right)}{\omega L_S}\sin\left(\omega t - \frac{\pi}{2}\right) \tag{3}$$

Where, V_m is the amplitude of v_{AC} and ω is its angular frequency.

Figure 2: The unipolar sinusoidal pulse width modulation triggering signals.



Initially, the capacitors C_{DC} and C_T started charging from the full-bridge rectifier (D_1D_4-D_3D_2). If at a certain time $t=t_0$, V_{DC} becomes slightly greater than V_{DCR}, then S_5 will be turned on causing D_6 to be turned off due to the declination of V_{DC} below the value of V_T. Assuming that S_5 and S_6 are triggered as shown in Figure 3, at the period defined by $t_0 \leq t \leq t_1$, the following can be written

$$V_{DCR} = L_{BU} \frac{di_1(t)}{dt} + R_{BU} i_1(t) \tag{4}$$

Solving (4) for $i_1(t)$ gives

$$i_1(t) = i_2(t) = \frac{V_{DCR}}{R_{BU}} \left(1 - \exp\left(-(t-t_0) \frac{R_{BU}}{L_{BU}} \right) \right) + i_1(t_0) \exp\left(-(t-t_0) \frac{R_{BU}}{L_{BU}} \right) \tag{5}$$

Since at $t=t_1$ S_5 is turned off, the energy stored in the inductor L_S is directed toward C_T. The charging of C_T at the period defined by $t_1 \leq t \leq t_2$, will be governed according to Kirchhoff Voltage Law, by the below differential equation

$$V_{DCR} = L_{BU} C_T \frac{d^2 V_T(t)}{dt^2} + R_{BU} C_T \frac{dV_T(t)}{dt} + V_T(t) \tag{6}$$

Solving (6) for the homogeneous solution $V_{TH}(t)$ gives

$$V_{TH}(t) = k_1 \exp\left(\frac{(t-t_1)}{2L_{BU}} \left(-R_{BU} - \sqrt{{R_{BU}}^2 - \frac{4L_{BU}}{C_T}} \right) \right) + k_2 \exp\left(\frac{(t-t_1)}{2L_{BU}} \left(-R_{BU} + \sqrt{{R_{BU}}^2 - \frac{4L_{BU}}{C_T}} \right) \right) \tag{7}$$

Where, k_1 and k_2 are constants. For this compensator ${R_{BU}}^2$ is usually smaller than $4L_{BU}/C_T$, thus $V_{TH}(t)$ represents an under damped case and the solution can be given by

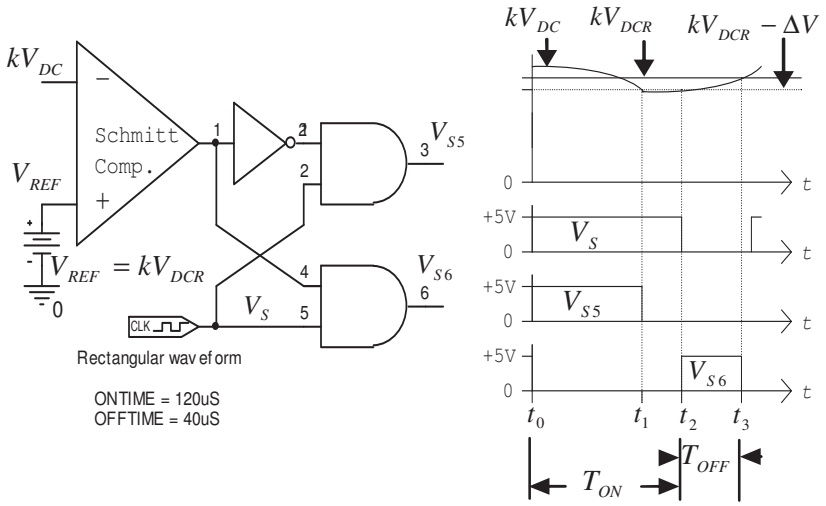
$$V_{TH}(t) = A_1 \cos\left(\omega_d (t-t_1) \right) e^{-(t-t_1)\alpha} + A_2 \sin\left(\omega_d (t-t_1) \right) e^{-(t-t_1)\alpha} \tag{8}$$

Where A_1 and A_2 are also constants and can be obtained from the initial conditions. α and ω_d are defined by

$$\alpha = R_{BU} / 2L_{BU} \tag{9}$$

$$\omega_d = \sqrt{1/L_{BU} C_T - \alpha^2} \tag{10}$$

Figure 3: S_5 and S_6 triggering technique.



The complete solution of (6) is the homogeneous solution $V_{TH}(t)$ plus the particular solution $V_{TP}(t)$ which is represented by V_{DCR}. Consequently, the complete solution of (6) can be given by

$$V_T(t) = V_{TH}(t) + V_{TP}(t) = A_1 \cos\left(\omega_d (t-t_1)\right) e^{-(t-t_1)\alpha} + A_2 \sin\left(\omega_d (t-t_1)\right) e^{-(t-t_1)\alpha} + V_{DCR} \tag{11}$$

The current $i_1(t)$ can be defined by

$$i_1(t) = -i_3(t) = C_T \frac{dV_T(t)}{t} = C_T\left(-\alpha A_1 + \omega_d A_2\right)\cos\left(\omega d (t-t_1)\right) e^{-(t-t_1)\alpha} - C_T\left(\omega_d A_1 + \alpha A_2\right)\sin\left(\omega d (t-t_1)\right) e^{-(t-t_1)\alpha} \tag{12}$$

Where, A_1 and A_2 are determined from initial conditions as follows

$$A_1 = V_T(t_1) - V_{DCR} \tag{13}$$

$$A_2 = \frac{\alpha C_T V_T(t_1) - \alpha C_T V_{DCR} + i_1(t_1)}{\omega_d C_T} \tag{14}$$

If V_{DC} is less than V_{DCR} at $t=t_2$, then the switch S_6 will conduct. In a procedure similar to that done in the period $t_1 \leq t \leq t_2$, the voltage $V_T(t)$ and the current $i_1(t)$ in the period $t_2 \leq t \leq t_3$ can be given by

$$V_T(t) = A_3 \cos\left(\omega_d (t-t_2)\right) e^{-(t-t_2)\alpha} + A_4 \sin\left(\omega_d (t-t_2)\right) e^{-(t-t_2)\alpha} + V_{DCR} \tag{15}$$

$$i_1(t) = -i_3(t) = C_T \frac{dV_T(t)}{t} = C_T\left(-\alpha A_3 + \omega_d A_4\right)\cos\left(\omega_d (t-t_2)\right) e^{-(t-t_2)\alpha} - C_T\left(\omega_d A_3 + \alpha A_4\right)\sin\left(\omega_d (t-t_2)\right) e^{-(t-t_2)\alpha} \tag{16}$$

Where, A_3 and A_4 are constants and can be obtained from the initial conditions as follows

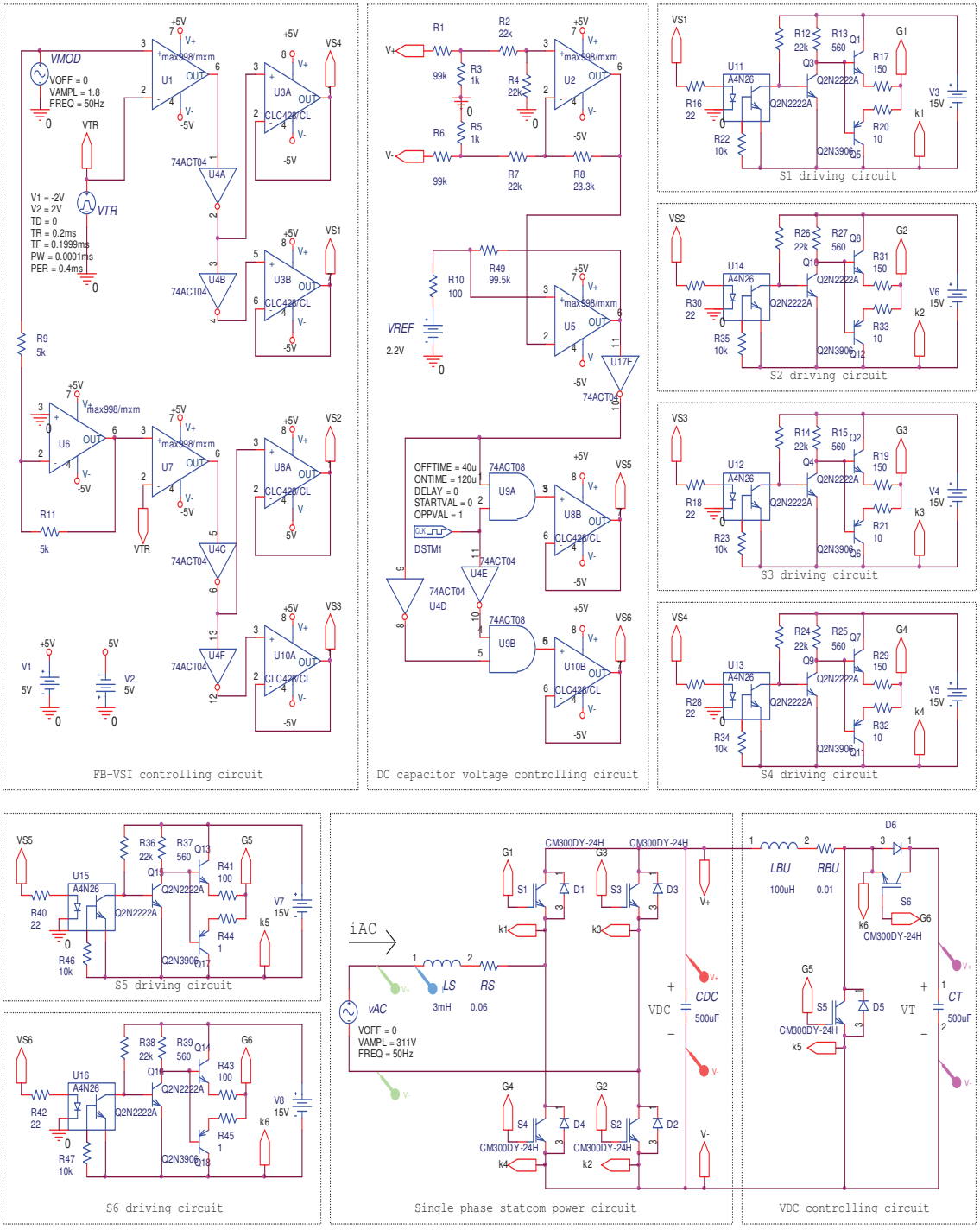
$$A_3 = V_T(t_2) - V_{DCR} \tag{17}$$

$$A_4 = \frac{\alpha C_T V_T(t_2) - \alpha C_T V_{DCR} + i_1(t_2)}{\omega_d C_T} \tag{18}$$

3. PSpice Validation System

Figure 4 shows a PSpice system demonstrating the design methodology and the objective of the proposed synchronous reactor. A power system of 220V, 50Hz was chosen as the AC supply v_{AC} for the proposed system. The carrier frequency f_C was chosen to be 2.5KHz, thus an inductance of 3mH was sufficient for L_S to suppress all the current harmonics running at the multiples of that frequency. The amplitude of v_{AC} was 311V. The FB-VSI was operated at a modulation index of 0.9. A linear adjustment of V_{DC} from 345V to 220V, was required to operate the synchronous reactor in a current range of 0 to 120A (peak values). C_{DC} and C_T were chosen to have equal capacitances of 500μF. The rectangular waveform voltage V_S was chosen to have a frequency of 6.25 KHz with T_{ON}=120μs and T_{OFF}=40μs.

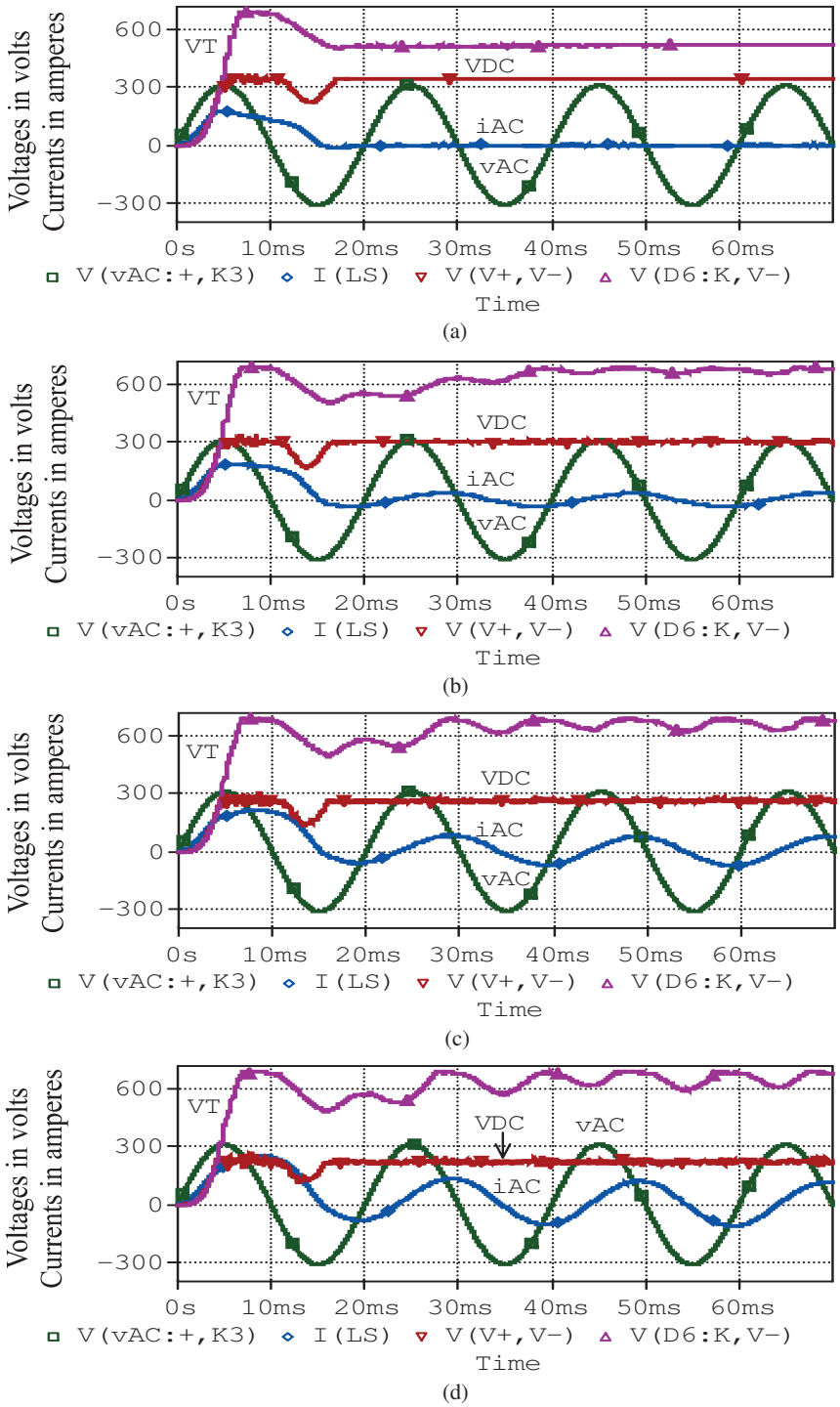
Figure 4: The PSpice validation system of the proposed synchronous reactor.



4. Results

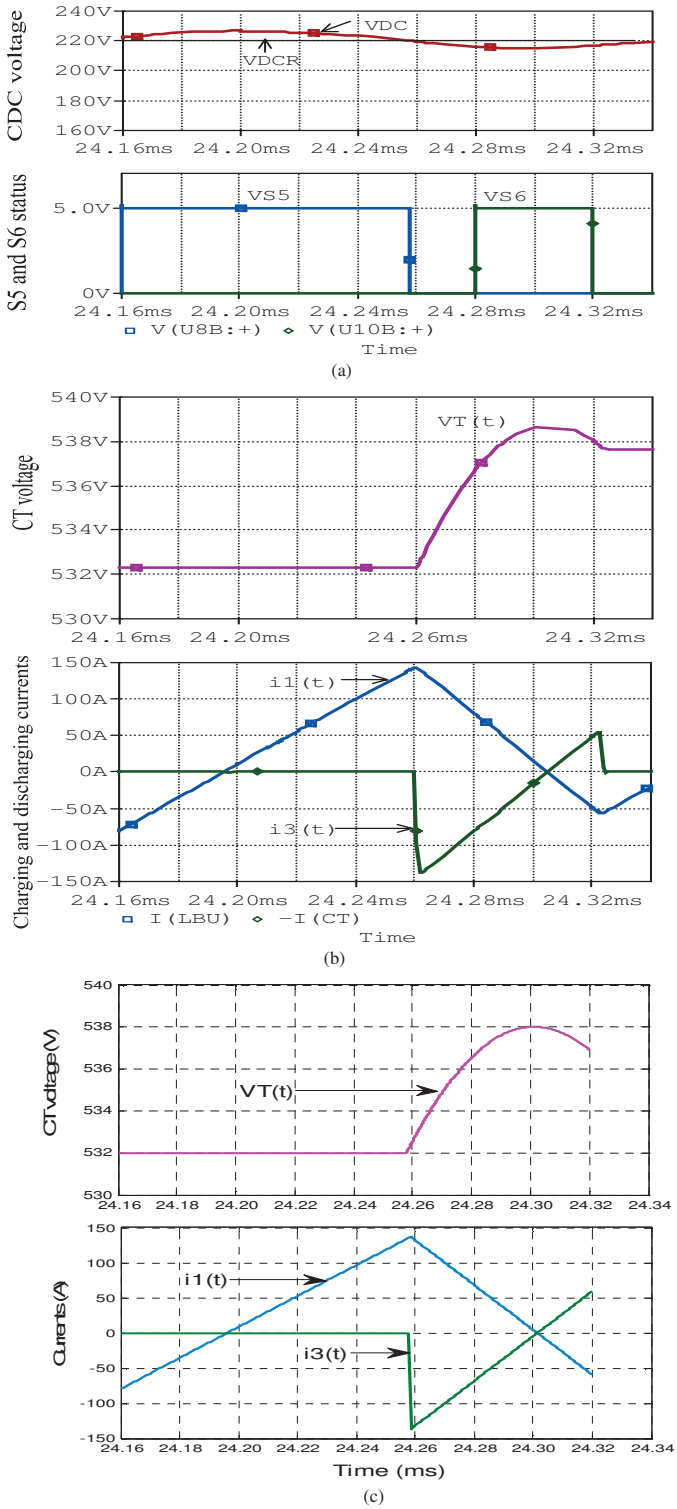
Fig. 5 shows the synchronous reactor performance at four different values of V_{DCR}. The capacitor voltage V_{DC} can be adjusted linearly by varying the reference voltage V_{REF} in Figure 4. Note that the electronic circuit was designed such that V_{REF}=kV_{DCR}=0.01V_{DCR}. The minimum V_{DCR} determines the maximum current rating of the reactor. V_{DCR} values of 345V, 303V, 262V, and 220V in Figure 5 are corresponding to source current i_{AC} of 0, 40A, 80A, and 120A respectively.

Figure 5: The AC voltage v_{AC}, reactor current i_{AC}, V_{DC}, and tank voltage V_T at V_{DCR} of: (a) 345V. (b) 303V. (c) 262V. (d) 220V.



To obtain the initial conditions and the time periods required for MATLAB simulation of (5), (11), (12), (15), and (16), a PSpice period defined by "24.16ms≤t≤24.32ms" was extracted from Figure 5d. Figure 6 shows PSpice and MATLAB results.

Figure 6: (a) Switching status of S_5 and S_6. (b) Pspice profiles of $V_T(t)$, $i_1(t)$, and $i_3(t)$. (c) MATLAB profiles of $V_T(t)$, $i_1(t)$, and $i_3(t)$.



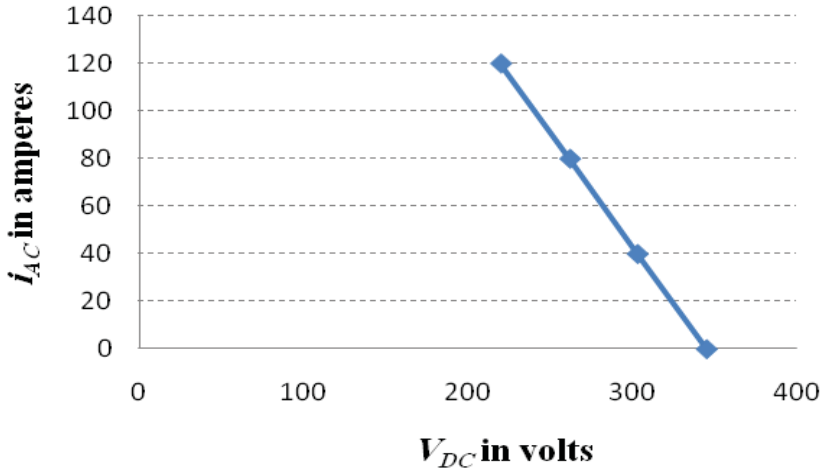
The switching status of S_5 and S_6 and the profiles of $V_T(t)$, $i_1(t)$, and $i_3(t)$ within that period are shown in Figure 6a and Figure 6b. From these figures, the following were obtained: t_0=24.16ms, t_1=24.258ms, t_2=24.28ms, t_3=24.32ms, V_{DCR}=220V, $V_T(t_0)$=532V, and $i_1(t_0)$=-80A. Figure 6c shows the MATLAB simulation results of (5), (11), (12), (15), and (16).

The linearity of the reactor current i_{AC} versus V_{DCR} is shown in Figure 7. Note that V_{DCR} is the average value of V_{DC} and the compensator in this paper was designed such that the maximum deviation

of V_{DC} from V_{DCR} never exceeds 2% of the minimum V_{DCR}. The Schmitt comparator is designed such that the switch S_5 is not allowed to conduct more than once within one cycle of V_S. As the difference between V_{DCR} and the AC supply amplitude V_m increases, the swing of V_{DC} from V_{DCR} increases too. The swing of V_{DC} from a V_{DCR} of 220V is within ±4.4V as shown in Figure 6a.

The coinciding of PSpice and MATLAB profiles of $V_T(t)$, $i_1(t)$, and $i_3(t)$ in Figure 6 validates the analysis carried out in this paper. The reactor represented by L_{BU} and R_{BU} was chosen such that its time constant is very much greater than the repetition time of the rectangular waveform V_S.

Figure 7: The synchronous reactor current i_{AC} versus C_{DC} voltage.



5. Summary and Concluding Remarks

The PSpice and MATLAB results have demonstrated the theoretical analysis of the proposed synchronous reactor. In addition, they reflect the linearity, harmonic absence, non-real power contribution, and pure reactive power absorption of the proposed compensator. The pure inductive current drawn by the proposed reactor from the AC supply ensures that the fundamental voltage component generated by the voltage source inverter is synchronized with the AC supply voltage. The proposed technique offers the possibility of using small series reactors without harmonic filtering or multilevel technology in inverter design. This is because of the precision regulation of the DC capacitor voltage, which is carried out without using external DC voltage sources. The technique offers the possibility of delta or star connections for reactive power absorption purposes. This reactor is characterized by very fast response (less than one cycle of the power system network fundamental) for satisfying the reactive current demand and negligible no load operating losses.

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