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Design of a Continuously Controlled Linear Static Var Compensator for Load Balancing and Power Factor Correction Purposes

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Abstract – *In this paper a new configuration of static Var compensator is presented. The configuration is a parallel combination of a binary thyristor switched-capacitor bank (BTSCB), a binary thyristor switched-reactor bank (BTSRB), and a thyristor controlled reactor (TCR). This compensator is capable of responding equally to both capacitive and inductive reactive current or reactive power demands for load balancing and power factor correction purposes. The harmonic contents of this configuration are almost ineffective, since the TCR which is the main source of them is only representing one seventh the compensator rating. Even though the BTSCB and BTSRB are offering stepping responses, the overall compensator response is linear since the TCR functions as a linearizer between adjacent steps in both capacitive and inductive modes of operation. This compensator is characterized by the possibility of operation at higher voltage and current ratings, low no load operating losses, and no need to harmonic filtering,. A complete system was designed and tested on the computer program PSpice.*

Keywords: *Load Balancing, Power Factor, Reactive Power Control, Static Var, Voltage Control*

Nomenclature

BTSCB	Binary thyristor switched-capacitor bank
BTSRB	Binary thyristor switched-reactor bank
TCR	Thyristor controlled reactor
V	a c line to line voltage
ω	ac voltage angular frequency
C	Capacitor bank basic capacitance
L	Reactor bank basic inductance
FC-TCR	Fixed capacitor-thyristor controlled reactor
i_{TCR}	Thyristor controlled reactor current
σ	Thyristor controlled reactor firing angle
V_F	Function circuit output voltage waveform
ADC	Analogue to digital converter
V_{in}	Compensator analogue input voltage
V_{ADC1}	Analogue input voltage of first analogue to digital converter
V_{TOG}	Toggling circuit triggering signal
i_{CB}	Capacitor bank instantaneous current
($D5$, $D6$, $D7$)	Most significant digits of the first analogue to digital converter
V_{ADC2}	Analogue input voltage of second analogue to digital converter
i_{LB}	Reactor bank instantaneous current
($D5^*$, $D6^*$, D^*7)	Most significant digits of the second analogue to digital converter
V_1	Analogue output voltage of the excessive capacitive current estimation circuit
V_2	Analogue output voltage of the deficient inductive current estimation circuit
V_3	Toggling circuit analogue output voltage
i_T	Compensator instantaneous total current
V_m	Line-to-line ac voltage amplitude

I. Introduction

Load balancing is employed for achieving better quality for power systems [1]. It requires continuous control of generation and absorption of reactive power [2]. Synchronous motors or condensers offer possibilities of continuous control of balanced reactive power generation, but they are characterized by very slow responses and high operating losses, therefore static Var compensators appeared as good replacements of them [3]. They are less expensive than synchronous condensers and characterized by fast responses and less operating losses, but they are still needing smooth controlling criteria associated with optimal operating losses [3], [4]. Fixed capacitor thyristor controlled reactor (FC-TCR) compensators can continuously generate a controllable reactive power, but they exhibit

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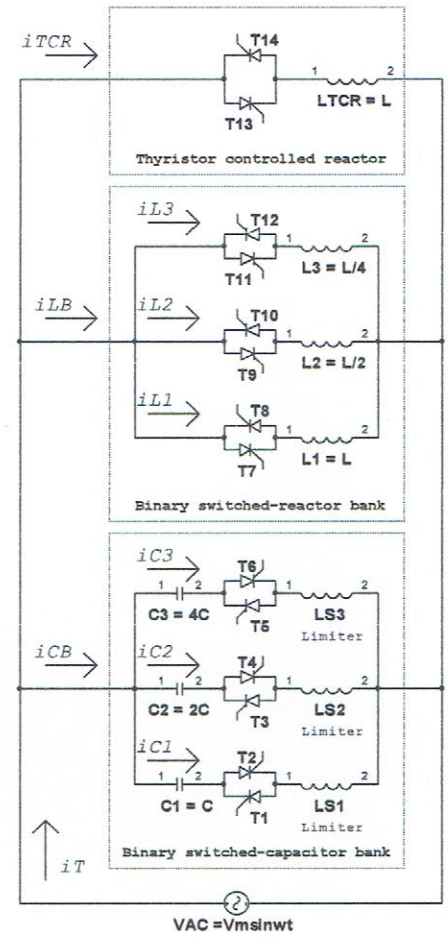
full load operating losses at no reactive power demand, since the TCR is operating at its full capacity in order to absorb the reactive power generated by the fixed capacitor [5]. The TCR is a source of harmonics, where the third harmonic for instance is about 13% of the TCR rating [4], [5]. This reveals the need for harmonics filters which add more complexity and more operating losses [6]. Switched-capacitor banks offer stepping responses in reactive power generation mode and their losses are proportional to the reactive power demands [7]. The above types of static Var compensators are called conventional types. They need medium speed solid state switching devices to function properly and hence they are less expensive [1]-[7]. A static compensator (STATCOM) which is basically built of a three phase converter shunted by a capacitor presents the feasibility of leading and lagging reactive power control [8]-[10]. This technique is restricted to low voltage applications, since it employs force-commutated fast solid-state switching devices having limited voltage and current ratings [11]. For linearity in both modes of compensation and higher voltage and current ratings purposes, an adaptive investment of conventional static Var compensators is presented in this paper for designing a new configuration responding continuously and linearly to capacitive and inductive reactive power or current demands with optimal reduction of no load operating losses and negligible harmonic contents.

II. The Proposed Configuration

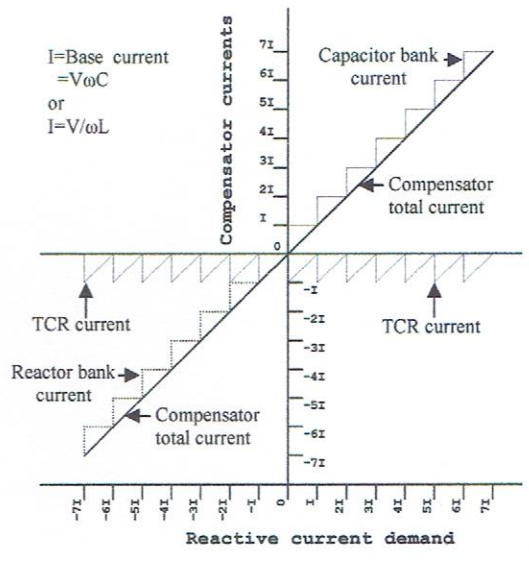
The proposed compensator is a new configuration. It is built of a binary thyristor switched-capacitor bank (BTSCB), a binary thyristor switched-reactor bank (BTSRB), and a thyristor controlled reactor (TCR). Fig. 1a shows this configuration. The BTSCB and BTSRB show stepping responses, while the TCR functions to set a linear overall response for the compensator as shown in Fig. 1(b). The TCR operates beside the BTSCB to cancel the excessive amount of capacitive reactive current and also operates with the BTSRB to compensate for the deficient inductive reactive current. The TCR rating is one seventh the BTSCB or BTSRB ratings which are $7V\omega C$ or $7V/\omega L$ respectively. Where V is the line-to-line voltage, C is the capacitor bank basic capacitance, L is the reactor bank basic inductance, and ω is the power system angular frequency. This means that ωC and $1/\omega L$ are equal.

In this work a single limb of three identical delta-connected limbs, is considered.

At slight capacitive reactive current demand, C_1 is switched on and the TCR is running at full load as stated in Fig. 1(b). This means that the no load operating losses and harmonic contents of this compensator are one seventh that of an equivalent conventional FC-TCR [4], [5]. The TCR current (i_{TCR}) in this compensator is a source of harmonics as shown in Fig. 2.



(a)



(b)

Figs. 1. The proposed compensator, (a) configuration, (b) performance scheme

Its fundamental as a function of the firing angle σ is given by [4]:

$$I = \frac{V}{\pi\omega L}(\pi - 2\sigma - sin2\sigma) \quad (1)$$

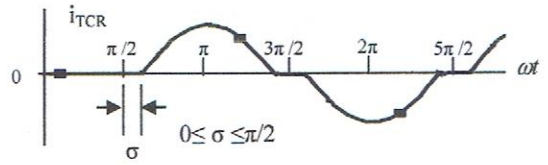


Fig. 2. The TCR current waveform

III. Proposed System Schematic Design

A schematic diagram of the proposed system is shown in Figs. 3. The power circuit is the same as that shown in Fig. 1(a).

The timing circuit produces five voltage waveforms responsible for managing the whole compensator and guaranteeing appropriate switching for capacitors and reactors.

Fig. 3(b) shows these waveforms. V_F represents the analogue simulation of the TCR fundamental component governed by Equation (1).

This compensator is excited by the analogue voltage V_{in} which is directly proportional to the reactive current demand. In this work, V_{in} is represented by a variable voltage source. +5V and -5V refer to maximum capacitive and inductive reactive current demands respectively.

The switched-capacitor bank triggering circuit is digitally controlled by the 8-bit analogue-to- digital converter (ADC1).

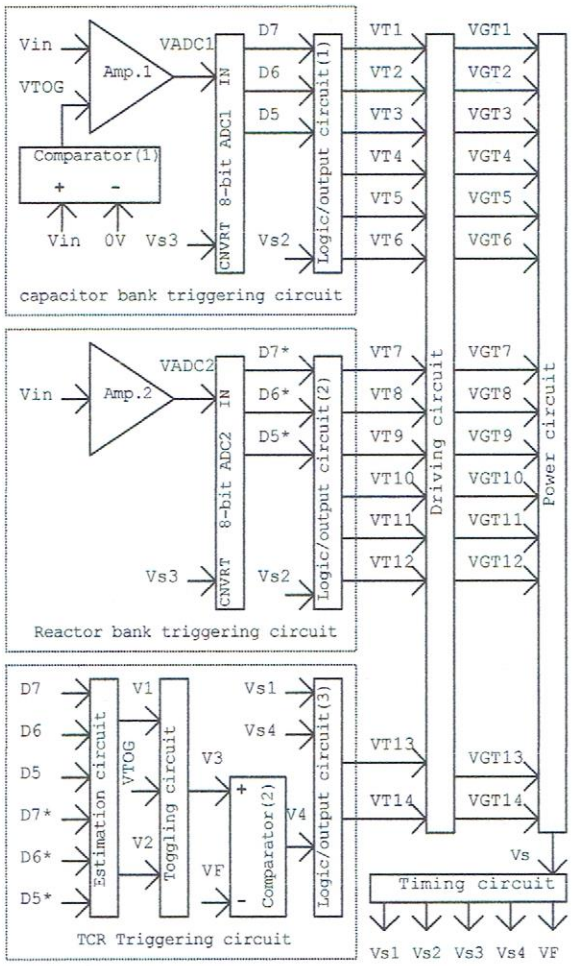
The input of ADC1 is set such that the response of this bank follows the stepping path shown in Fig. 1(b). Consequently, for values of V_{in} greater than zero, the analogue input of ADC1 is related to V_{in} as follows:

$$V_{ADC1} = \frac{14}{8}\left(V_{in} + \frac{V_{TOG}}{7}\right) \quad (2)$$

where V_{TOG} is +5V for V_{in}>0 and 0V for V_{in}≤0. The capacitor bank current (i_{CB}) is determined by the logic status of the three most significant digits ($D7$, $D6$, and $D5$) of ADC1 as follows:

$$i_{CB} = \omega C V_m \, sin\left(\omega t + \frac{\pi}{2}\right)\left[\frac{4D7}{5} + \frac{2D6}{5} + \frac{D5}{5}\right] \quad (3)$$

where V_m is the amplitude of line-to- line voltage V. For $D7$, $D6$, and $D5$, logic one corresponds to +5V and logic zero refers to 0V.



Figs. 3 The proposed compensator, (a) schematic design, (b) basic waveforms

The switched-reactor bank triggering circuit is designed such the reactor bank response follows the stepping path stated in Fig. 1(b).

Therefore the analogue input of ADC2 is related to V_{in} by:

$$V_{ADC2} = -\frac{14}{8}V_{in} \quad (4)$$

The reactor bank current (i_{LB}) is given as a function of the most significant digits ($D7^*$, $D6^*$, and $D5^*$) of ADC2:

$$i_{LB} = \frac{V_m}{\omega L}\sin\left(\omega t - \frac{\pi}{2}\right)\left[\frac{4D7^*}{5} + \frac{2D6^*}{5} + \frac{D5^*}{5}\right] \quad (5)$$

The conduction status of both capacitor and reactor banks are determined according to Table I and Table II respectively. A complete system following the schematic design steps, is implemented on the computer program PSpice as shown in Fig. 4.

Datasheets concerning all the electronic parts and aiding literatures were considered in this work [12]-[15]. The PSpice system is designed such that the capacitor bank and reactor bank are governed by the data given in Table I and Table II respectively.

In addition, the electronic circuit is designed such that the input of ADC2 is negative when V_{in} is greater than zero and the input of ADC1 is negative when V_{in} is less than zero.

This means that the capacitor bank triggering circuit will not respond during inductive reactive current demand and the reactor bank triggering circuit will not respond during capacitive reactive current demand.

TABLE I
CAPACITOR BANK SWITCHING STATUS FOR $0 \le V_{in} \le 5V$

V_{in} (V)	V_{ADC1}(V)	C_1 status	C_2 status	C_3 status
0	0	OFF	OFF	OFF
0^+	1.25	ON	OFF	OFF
0.71428	2.5	OFF	ON	OFF
1.42856	3.75	ON	ON	OFF
2.14284	5	OFF	OFF	ON
2.85712	6.25	ON	OFF	ON
3.57140	7.5	OFF	ON	ON
4.28568	8.75	ON	ON	ON
5	10	ON	ON	ON

TABLE II
REACTOR BANK SWITCHING STATUS FOR $-5V \le V_{in} \le 0$

V_{in} (V)	V_{ADC2}(V)	L_1 status	L_2 status	L_3 status
0	0	OFF	OFF	OFF
-0.71428	1.25	ON	OFF	OFF
-1.42856	2.5	OFF	ON	OFF
-2.14284	3.75	ON	ON	OFF
-2.85712	5	OFF	OFF	ON
-3.57140	6.25	ON	OFF	ON
-4.28568	7.5	OFF	ON	ON
-5	8.75	ON	ON	ON

The TCR current is determined by the status of the capacitor bank and the inductor bank currents.

For the case of capacitive reactive current demand, the capacitor bank is expected to be ready for supplying the reactive current demand, but its current will rather be excessive according to its response path shown in Fig. 1(b).

The estimation circuit will produce an analogue voltage V_1 proportional to that excess and is computed as follows:

$$V_1 = 7\left(\frac{4}{7}D7 + \frac{2}{7}D6 + \frac{1}{7}D5 - V_{in}\right) \quad (6)$$

Similarly, when the reactive current demand is inductive, the reactor bank will respond, but its current is rather insufficient to satisfy the demand. Again the estimation circuit produces an analogue voltage V_2 proportional to the deficient inductive reactive current demand and is computed as follows:

$$V_2 = 7\left(-\frac{4}{7}D7^* - \frac{2}{7}D6^* - \frac{1}{7}D5^* - V_{in}\right) \quad (7)$$

The output of the toggling circuit V_3 is toggled to V_1 when $V_{in}>0$ and to V_2 when $V_{in}\le 0$. Comparator (2) determines the TCR firing angle by comparing V_3 with V_F which governs the fundamental component of i_{TCR}. When $V_3>V_F$, then the comparator output is logic one and is zero else where. The compensator total current i_T is given by:

$$i_T = \begin{cases} i_{CB} + i_{TCR}, & V_{in} > 0 \\ i_{LB} + i_{TCR}, & V_{in} \le 0 \end{cases} \quad (8)$$

IV. Results and Discussion

The PSpice implementation of the system shown in Fig. 4 has the following basic design parameters: C=100μF, L=99.4mH, V_m=587V at a frequency of 50Hz. All performance tests were carried out at 27C°. In case of no reactive current demand (V_{in}=0), no sign of significant current appears in any branch of the power circuit since the BTSCB, BTSRB, and TCR are relaxed according to the control strategy of this compensator. In case of slight capacitive reactive current demand or definitely the case at which $V_{in}=0^+$ in Table I, only the capacitor C_1 is expected to be switched on.

This action will stimulate the TCR to exhibit its full capacity cancelling the excess of capacitive current detected by estimation circuit. Fig. 5 shows a test demonstrating the above condition. Note that the current flowing in the capacitor C_1 (i_{C1}) and i_{TCR} cancelled each other setting a zero i_T.

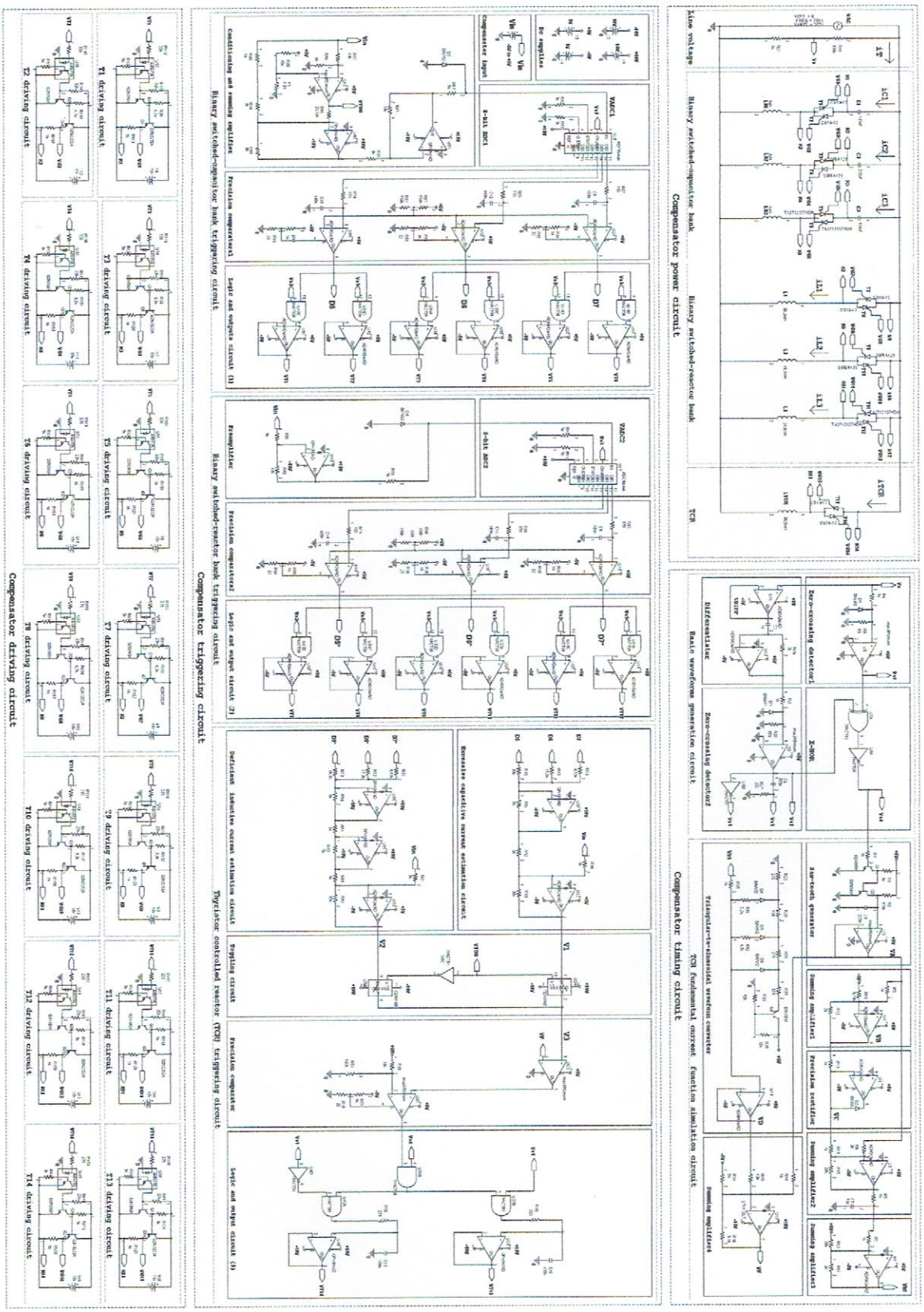


Fig. 4. The continuously controlled linear static Var compensator circuit diagram

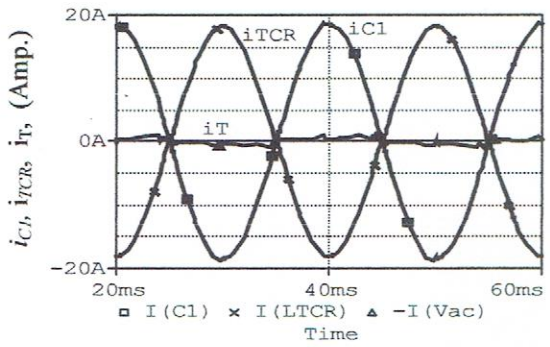
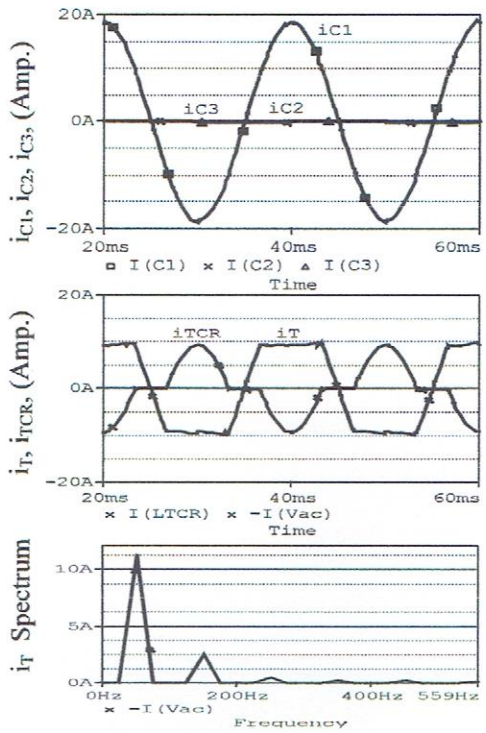


Fig. 5. Compensator status during slight capacitive current demand

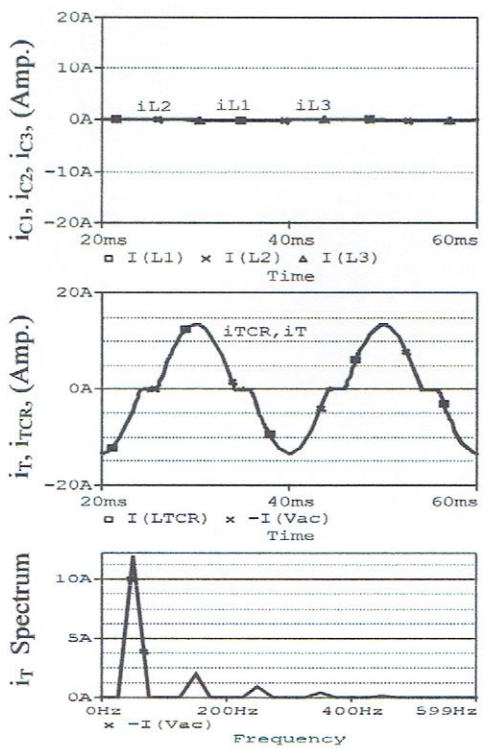
The compensator was also tested at 10% of its rating for both modes of operation. The corresponding values for V_{in} were +0.5V for capacitive reactive current demand and -0.5V for inductive reactive current demand. For the case of capacitive reactive demand, the capacitor C_1 was switched on according to Table I supplying a reactive current of about 18.5A (peak value) which exceeded the reactive current demand by 5.6A. Consequently, the TCR was activated to absorb that excess of capacitive current as shown in Fig. 6(a). For the case of inductive current demand, only the TCR responded to that demand as shown in Fig. 6(b). Even though the compensator total current waveforms in Figs. 6 seem somewhat non-sinusoidal, their harmonic contents are almost ineffective compared to their fundamentals.

Many tests were proceeded to check compensator linearity, switching status of power circuit, and the harmonic contents at various capacitive and inductive current demands. Figures 7, 8, 9, 10 and 11 correspond to compensator performance at 20%, 40%, 60%, 80% and 100% of its rating respectively. Examining these figures, leads to a conclusion that harmonic contents are vanishing compared to compensator actual current during the increasing of reactive current demand for both modes of operation (capacitive and inductive). The dominant harmonics generated by the TCR are the third, fifth, seventh, and ninth harmonics. These harmonics were measured through many tests and no one of them touched a value of 2% of the compensator rating in both capacitive and inductive modes of operation. Theoretically, no one of harmonics in this compensator will exceed 2% of the compensator rating, since the TCR rating which is the source of them is one seventh the compensator rating.

Generally, in all tests the compensator performance follows the control strategy specified in Table I, Table II, and the estimation circuit. The overall performance of this compensator is shown in Fig. 12(a) where linearity is demonstrated within the predetermined area of operation. Fig. 12(b) shows the harmonic contents as percentages of compensator rating. Figs. 12 present this compensator as a productive tool in power quality improvement.

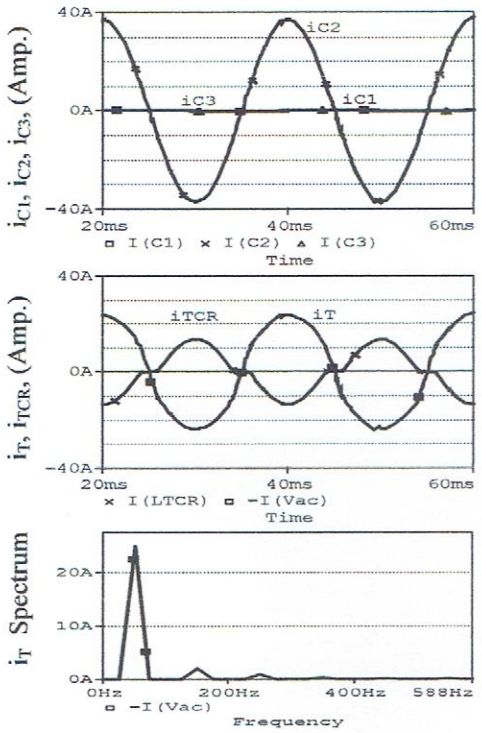


(a)

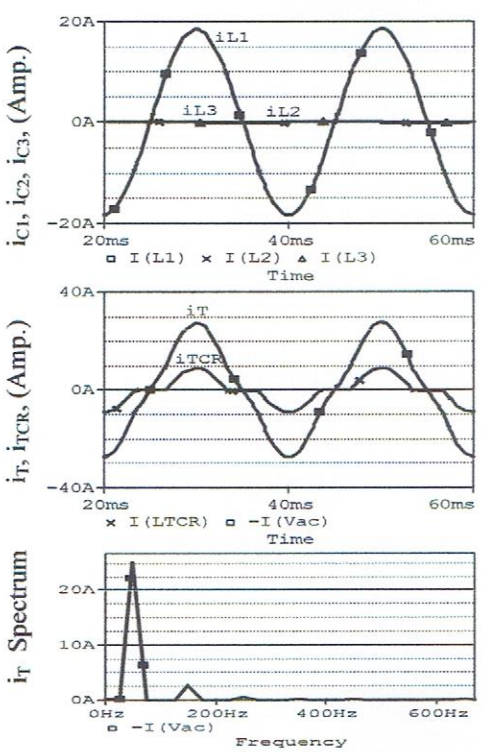


(b)

Figs. 6. Compensator response during 10% of its rating, (a) capacitive reactive current demand, (b) inductive reactive current demand

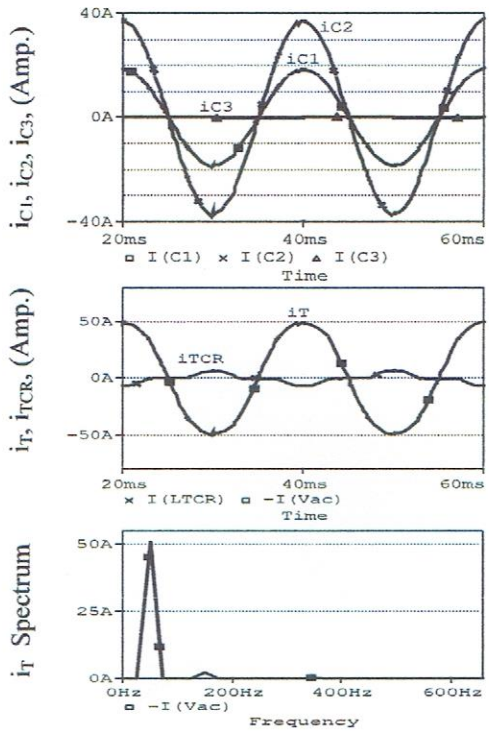


(a)

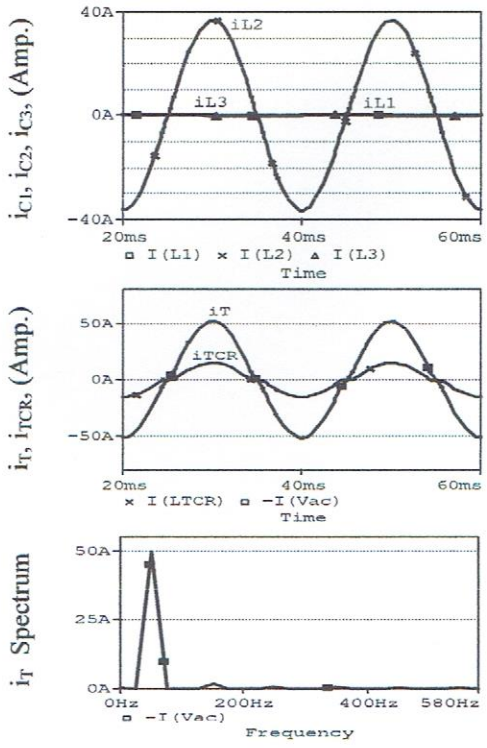


(b)

Figs. 7. Compensator response during 20% of its rating, (a) capacitive reactive current demand, (b) inductive reactive current demand

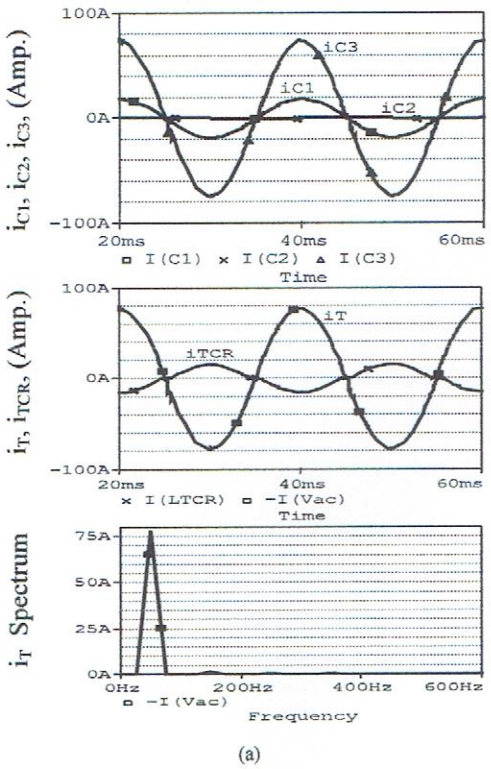


(a)

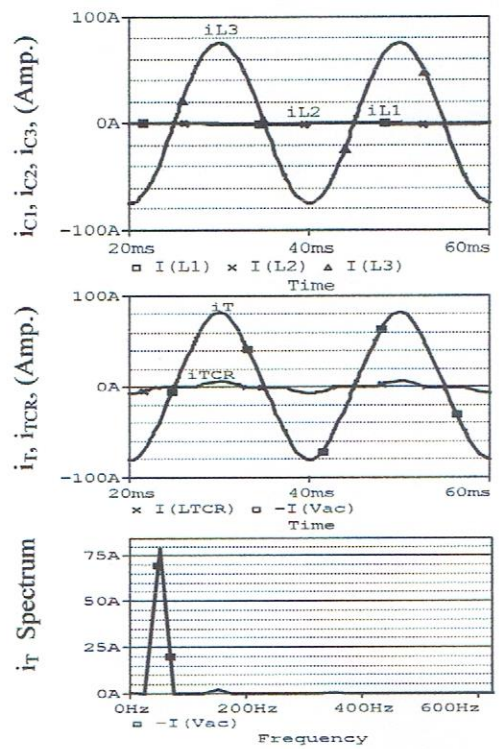


(b)

Figs. 8. Compensator response during 40% of its rating, (a) capacitive reactive current demand, (b) inductive reactive current demand

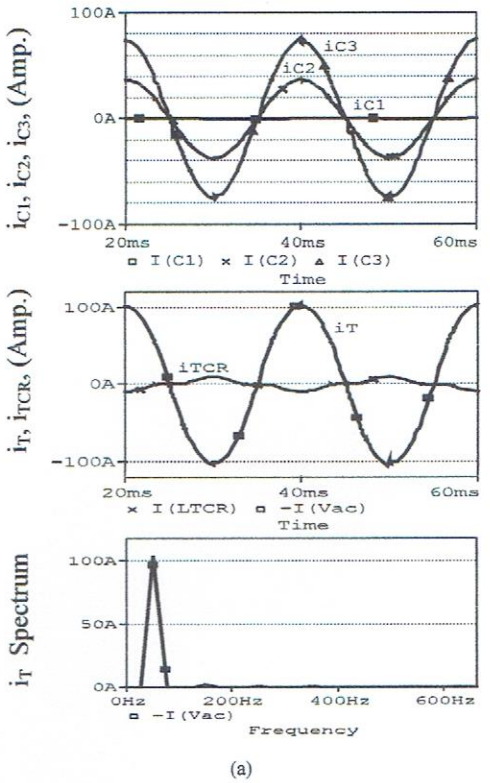


(a)

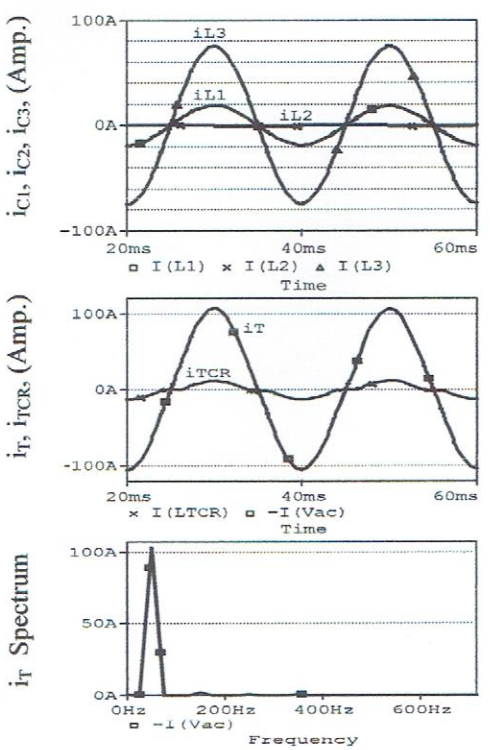


(b)

Figs. 9. Compensator response during 60% of its rating, (a) capacitive reactive current demand, (b) inductive reactive current demand

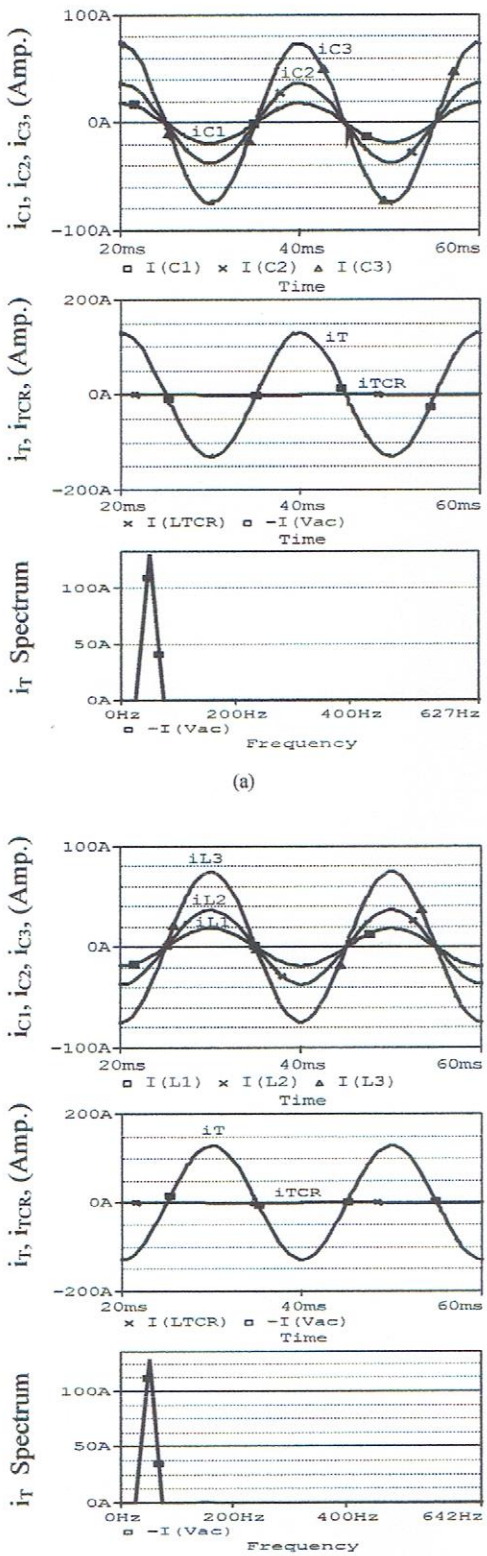


(a)

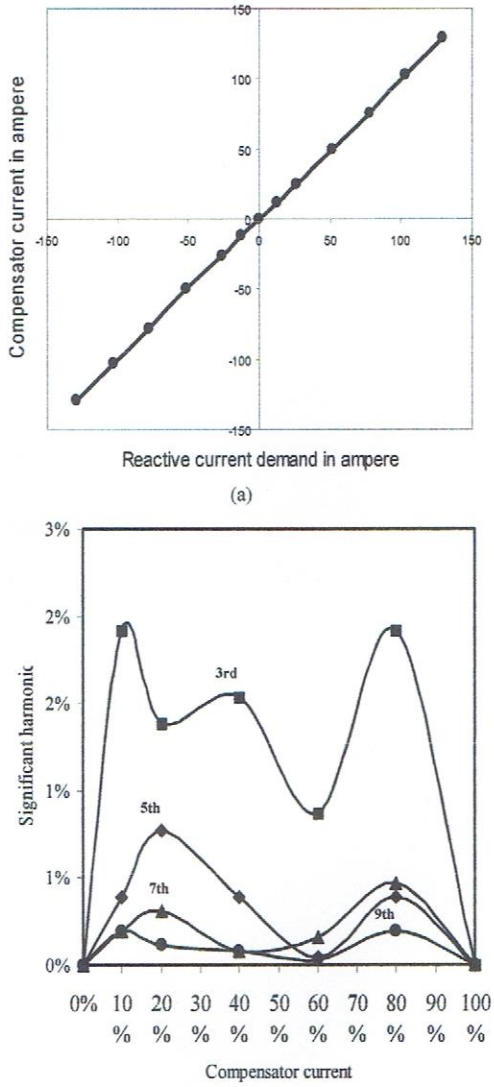


(b)

Figs. 10. Compensator response during 80% of its rating, (a) capacitive reactive current demand, (b) inductive reactive current demand



Figs. 11. Compensator response during 100% of its rating, (a) capacitive reactive current demand, (b) inductive reactive current demand



Figs. 12. Compensator overall performance, (a) linearity, (b) harmonic contents

V. Conclusion

In this paper a single limb of a three phase compensator is designed and tested on PSpice. The three phase configuration can easily be constructed by connecting three identical limbs in delta form, installing a measuring circuit for detecting line voltages and currents, and adding a computational circuit for processing the detected voltage and current signals so as to create three controlling inputs V_{in1}, V_{in2}, and V_{in3}. Basically, each one of these controlling signals will determine the reactive current demand for a single limb. The response of a single limb or a three phase configuration to sudden changes of reactive current demands can be settled within less than a cycle of power

system frequency, since necessary computations will be accomplished at the beginning of the second quarter of each line voltage cycle. This compensator needs no harmonic filtering; therefore it is less complicated, less dissipative, and less expensive. In addition, the compensator exhibits minimal no load operating losses compared to an equivalent FC-TCR compensator. Linearity of this compensator and feasibility of operating it at higher voltage and current ratings, assures adopting it as a competitive tool amongst load balancing techniques for achieving better power quality improvement.

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Acknowledgements

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