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Design of a Three-phase Voltage Regulator Equipped with Voltage Balancing Technique

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Abstract

This paper presents a controlling strategy based on the addition of three reactive T-section circuitries connected in series with a star-connected 3-phase load impedance. The left hand side branch of each T-section is a pure inductance having a constant reactance of +jX, while the right hand side impedance is a pure capacitance having a constant reactance of –jX. The middle branch is a susceptance B, which is composed of a switched capacitor bank in shunt with a switched inductor and is connected to the star point of the load impedance. This susceptance is controllable in the range of ±Bmax. The system is capable of maintaining the three-phase load voltage at its rated value even though the power system voltage is varying within the range of 80% to 120% of its rated value. In addition, the system is equipped with voltage balancing technique and is almost free from harmonics. The whole system was designed and implemented using PSpice Program.

الخلاصة

في هذا البحث تم تقديم طريقة جديدة للسيطرة على منظم فولتية ثلاثي الطور باستخدام ثلاثة دوائر كهربائيـة كـل منها على شكل حرف **T** وتربط الدوائر الثلاثة على شكل النجمة بين الحمل ومصدر القدرة. الجزء الأيسر من كـل دائـرة عبارة عن محاثة نقية راداتها الحثية jX+ والجزء الأيمن عبارة عن متسعة نقية راداتها السعوية jX- بينما الجزء الوسـطي عبارة عن مسامحة **B** تتألف من بنك متسعات مفتاحي على التوازي مع محاثة مفتاحية. يمكن السيطرة على قيمتها ضـمن المدى ±Bmax . النظام قادر على إبقاء فولتية الحمل ضمن معدلاتها حتى لو تغيرت فولتية المصدر ضمن المـدى ٨٠% الى ١٢٠% من معدلاتها. بالإضافة إلى ذلك يستطيع النظام موازنة فولتية الحمل وإبقائها ضمن معدلاتها حتـى لـو كانـت فولتية المصدر الثلاثي الطور غير متوازنة. النظام غير منتج للتوافقيات تقريبا وتم تصميمه وتنفيـذه باسـتخدام البرنـامج ألتشبيهي (**PSpice**).

1. Introduction

Voltage regulators play an important role in the preparation of the environments for proper operation of electrical equipments. They are graded from the primitive forms of control such as the tab changing transformers equipped with servo-mechanism to the more complicated systems which are accomplished by controlling the reactive power of the ac power system using more advanced technologies (Rahman and Shahidehpour 1994, Yoshida et al 1999, Bimal 2006, Benslimane et al 2006, Kalyani and Das 2007, Pachar and Tiwari 2008). Reactive power control is achieved by using static var compensators which treat system voltage fluctuations (Valderrama et al 2001, Li et al 2006). These compensators are employing static switching devices for connecting reactive passive components to the power system network. Variable inductors are used to absorb reactive power from the power system network for the sake of lowering the system voltage, while switched capacitor banks are used for raising the system terminal voltage (Benslimane et al 2006, Kalyani and Das 2007). Here in this paper, an adaptive technique is adopted to control the system terminal voltage by employing an additional circuitry to the system for the sake of bringing the load voltage to its rated value. The proposed system offers an adaptive environment for electrical loads even though the

power system is suffering undesirable voltage fluctuations. In addition, the system under discussion is convenient for various electrical energy consumers, since it presents a reliable technology for balancing the three-phase load voltage.

2. The proposed voltage regulation approach

Fig. 1 shows a single-phase circuit of the proposed regulator. B is a reactive variable susceptance and it is either capacitive or inductive depending upon the input voltage status. For instance, if the input voltage is below the load rated voltage V_L, then B will be identified to be capacitive and its value is determined such that the load voltage is raised to its rated value. When the input voltage is above the load rated value, B will be inductive susceptance of a value capable of reducing the load voltage to its rated value.

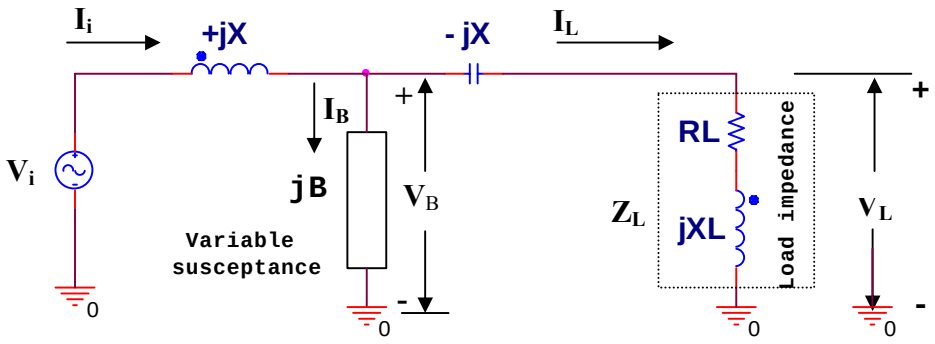


Fig. 1 Single-phase circuit of the proposed regulator.

Fig. 2 shows phasor diagrams indicating the above criteria. Note that V_i and V_L are looking in phase. The voltage V_B and the compensating current I_B are given by

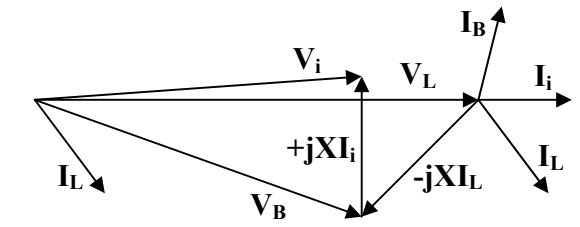
$$V_B = -jXI_L + V_L \quad \text{..... (1)}$$

$$I_B = jBV_B$$
$$= BXI_L + jBV_L \quad \text{..... (2)}$$

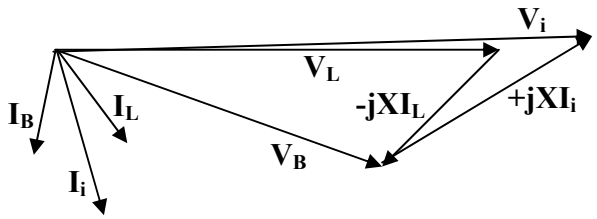
Referring to **Fig. 2**, the input current I_i and the input voltage V_i are given by

$$I_i = I_L + I_B$$
$$= I_L(1 + BX) + jBV_L \quad \text{..... (3)}$$

$$V_i = jXI_i + V_B$$
$$= jX^2 I_L B + V_L(1 - XB) \quad \text{..... (4)}$$



(a)



(b)

Fig. 2 Single-phase regulator phasor diagrams; (a) V_i is less than the rated voltage V_L, (b) V_i is greater than V_L.

The load voltage V_L is taken as a base and reference voltage and is decided to be maintained at its rated value. If the reactance X is chosen to be 20 percent of the absolute value of the rated load impedance $|Z_{Lrated}|$, then Equation (4) can be rewritten as:

$$V_i = j0.04|Z_{Lrated}|^2 I_L B + V_L\left(1 - 0.2|Z_{Lrated}|B\right) \quad \text{..... (5)}$$

If the maximum value of |B| is chosen to be $(1/|Z_{Lrated}|)$, then the factor $|Z_{Lrated}|B$ is either equal or less than unity. In addition, $I_L|Z_{Lrated}|$ is always equal or less than the rated voltage V_L. Consequently, Equation (5) can be very closely approximated to:

$$V_i = V_L\left(1 - 0.2|Z_{Lrated}|B\right) \quad \text{.....(6)}$$

Since B is either capacitive or inductive, its value is either positive or negative respectively. **Equation (6)** shows that Vi is in phase with V_L and can be controlled within the range of $0.8V_L$ to $1.2V_L$. Note that **Equation (6)** is valid for both resistive and inductive loads and will be more accurate when the load current is below its rated values. The controlling susceptance can be equated to:

$$B = -5\left(\frac{V_i - V_L}{\frac{V_L}{|Z_{Lrated}|}}\right) \quad \text{.......................................} \quad (7)$$

Equation (7) is employed as the basic regulator controlling criterion for both single-phase and three-phase configurations. Positive values of B indicate that V_i is less than V_L and the required susceptances is capacitive, while negative values indicate that V_i exceeds V_L and the required susceptance is inductive. The capacitive susceptance is produced by a switched capacitor bank controlled in a stepping manner from C to15C, where C is the base capacitance or the capacitance step. Inductive susceptance is generated by shunting the switched capacitor bank by a switched inductor having inductance of $1/15\omega^2C$, where ω is the ac voltage angular frequency. Operating the switched inductor with appropriate switched capacitors will achieve the inductive susceptance demand.

2. 1 Single-phase configuration

Fig. 3 shows the single-phase configuration of the proposed regulator. The switched capacitor bank is composed of four switched capacitors having values of C, 2C, 4C, and 8C. The corresponding switches of these capacitors are controlled by the output digits of 4-bit analogue-to-digital converter. The switched inductor will be operated when the phase input voltage exceeds the rated value and hence certain switched capacitors will be operated together with the switched inductor to guarantee the required inductive susceptance. The required reactive susceptance variations against the normalized input phase voltage change $(V_i-V_L)/V_L$ are shown in **Fig. 4**.

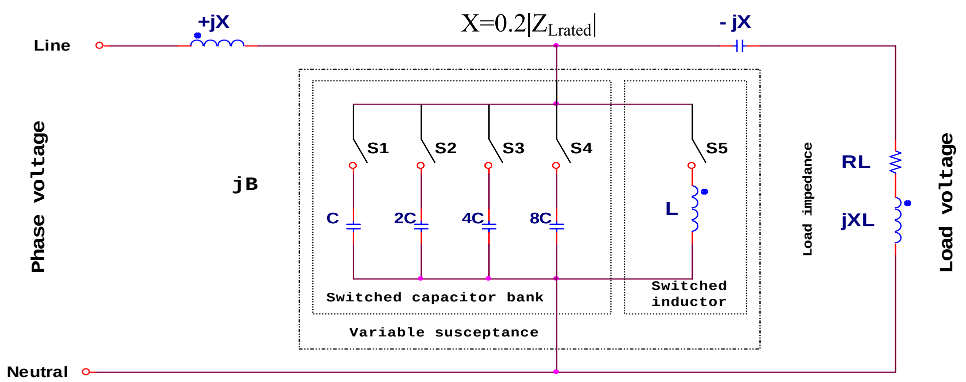


Fig. 3 Proposed regulator single-phase configuration.

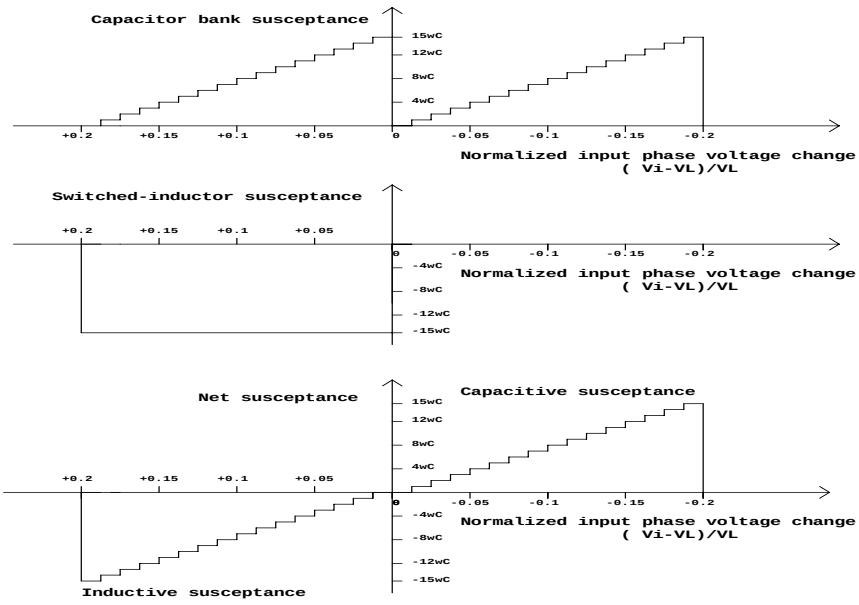


Fig. 4 Susceptance variations with the normalized input phase voltage change.

2. 2 Three-phase configuration

The three-phase configuration of the proposed regulator is shown in **Fig. 5**. There are three star-connected identical susceptances. Here the three-phase load impedance is not assumed to be balanced. Consequently such type of regulators is convenient for a wide variety of loads. The three-phase input voltages are not assumed to be balanced.

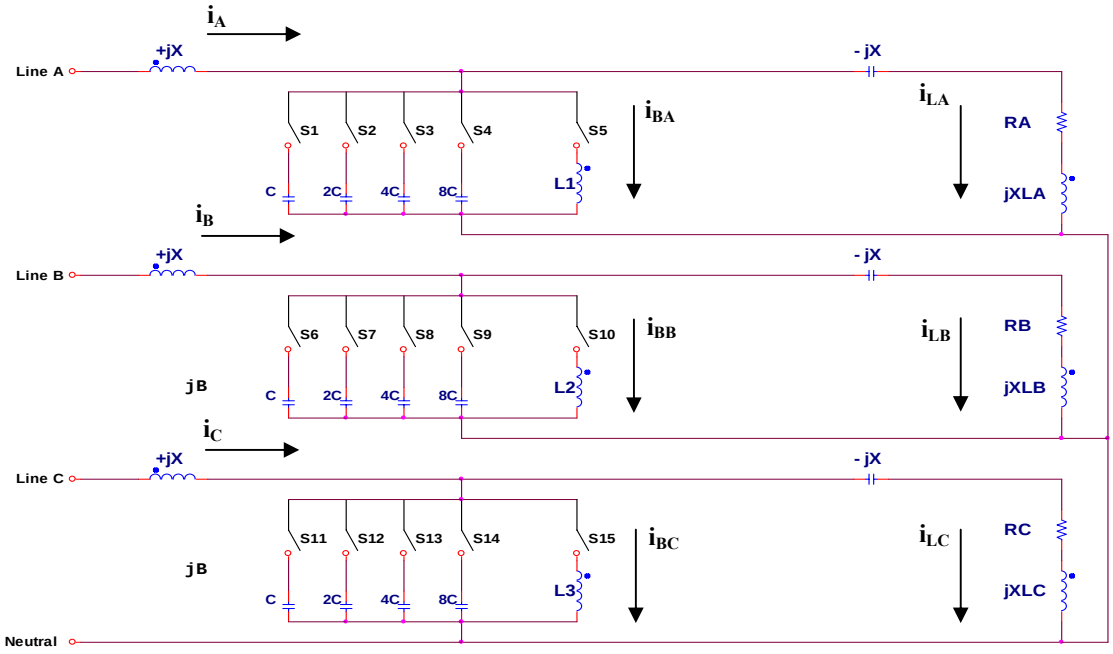


Fig. 5 Three-phase configuration of the proposed regulator.

3. The three-phase regulator schematic design

The schematic design of a complete system is shown in **Fig. 6**. The system is designed such that it can supply balanced and rated three-phase voltage even though the input three-phase voltage is not balanced in amplitude. Here the three-phase input voltage is assumed to be phase balanced. The controlling circuit of this system consists of three similar sub circuits. Each sub circuit steps down the phase voltage through the potential divider to the level such that the peak detector output will be +5V when the input phase voltage is at its rated value (220V rms). The difference amplifier subtracts the peak detector output from the dc voltage V_{REF1} and multiplies the resultant by 2. V_{REF1} is +5V.

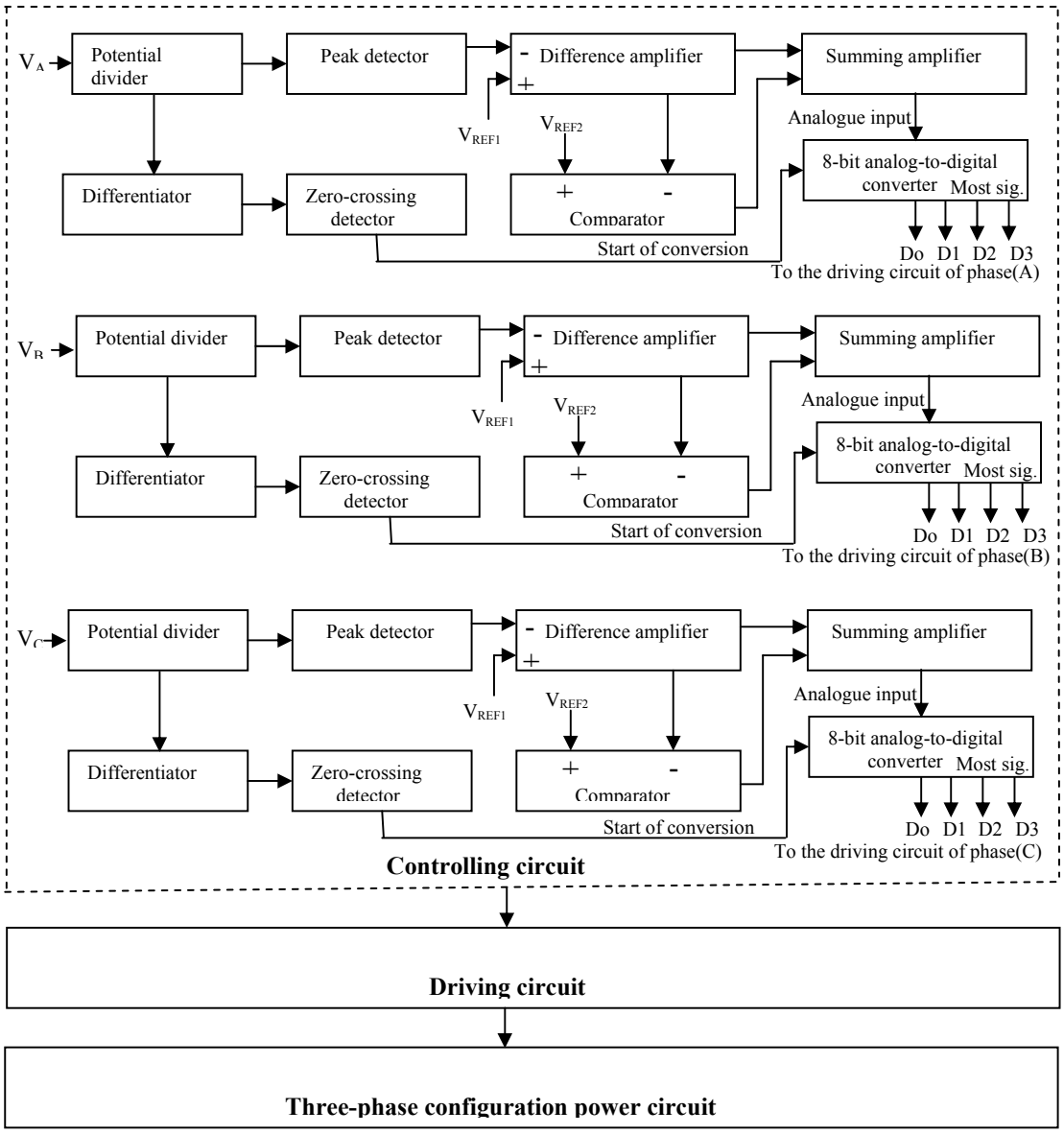


Fig. 6 The proposed three-phase regulator schematic design.

When the input phase voltage varies within the range of ($0.8V_L$ to $1.2\ V_L$), the corresponding output of the difference amplifier will be in the range of (+10V to -10V). The positive values of this output denote that the required susceptances are capacitive, while the negative values refer to inductive susceptances. If the difference amplifier output is more positive than V_{REF2} which is a dc voltage of –o.625V, the output of the comparator will be zero leading the summing amplifier to produce the same output of the difference amplifier. Consequently the 4-bit analog-to-digital converter will convert the latter dc voltage to digital. The 4-bit analog-to-digital converter digital outputs are all high for 10 volts dc input and are all low for zero input. Note that Do triggers the switch of the C capacitor, D1 triggers the switch of the 2C capacitor, D2 triggers the switch of the 4C capacitor, and D3 triggers the switch of the 8C capacitor. When the difference amplifier output is less negative than -0.625V, the comparator output will be +10V enabling the controlling signal VSL to switch on the switched-inductor which produce a negative susceptance of -15ωC. The summing amplifier output in this case, is a dc voltage proportional to the capacitive susceptance required to cancel the excessive inductive susceptance. For example, a -5V at the output of the difference amplifier points to a required inductive susceptance of (-8ωC), but the switched inductor injects an inductive susceptance of (-15ωC) which exceeds the required susceptance by an amount of (-7ωC). Here the summing amplifier output is 5V leading D3 of the 4-bit analog-to-digital converter to go high switching on the 8C capacitor which adds a capacitive susceptance of (8ωC). The net generated susceptance is (-7ωC) which differs from the required inductive susceptance by (-1ωC). The associative effect of this error on the compensated load voltage will not exceed 2 percent at full load. When the output of the difference amplifier is within the range of (-0.625V to +0.625V), both the switched capacitor bank and the switched-inductor are not triggered and load phase voltage will coincide with the input phase voltage leading to a maximum expected error of less than 2 percent. The driving circuit includes an individual driving circuit for each switching device which isolates the controlling signal from the power circuit and offers the proper switching performance of the switching device. The power circuit here is the three phase configuration shown in **Fig. 5**. This circuit is star-connected. The over all function of this regulator is to regulate the load voltage to its rated value and performs voltage balancing when the input three-phase voltage is not balanced.

4. Regulator circuit diagram

The complete system is designed and implemented on PSpice. **Fig. 7** shows the complete circuit diagram of this system which follows the steps of the schematic design shown in **Fig. 6**. Datasheets of all the electronic parts and many assisting literatures were invested throughout the design process (Malmstadt et al 1981, Millman and Halkias 1983, Rashid 2001, Skvarenina 2001, Acha et al 2002). It is recommended here to concern the building circuits of this system individually in order to exhibit their functions obviously. The controlling circuit of the implemented system consists of three identical categories. Each one of them concern one phase. The whole driving circuit of this system includes eighteen almost identical driving circuits which were designed according to the datasheets of the switching devices employed in this regulator. Finally, the three-phase power circuit includes three identical circuits connected in star form.

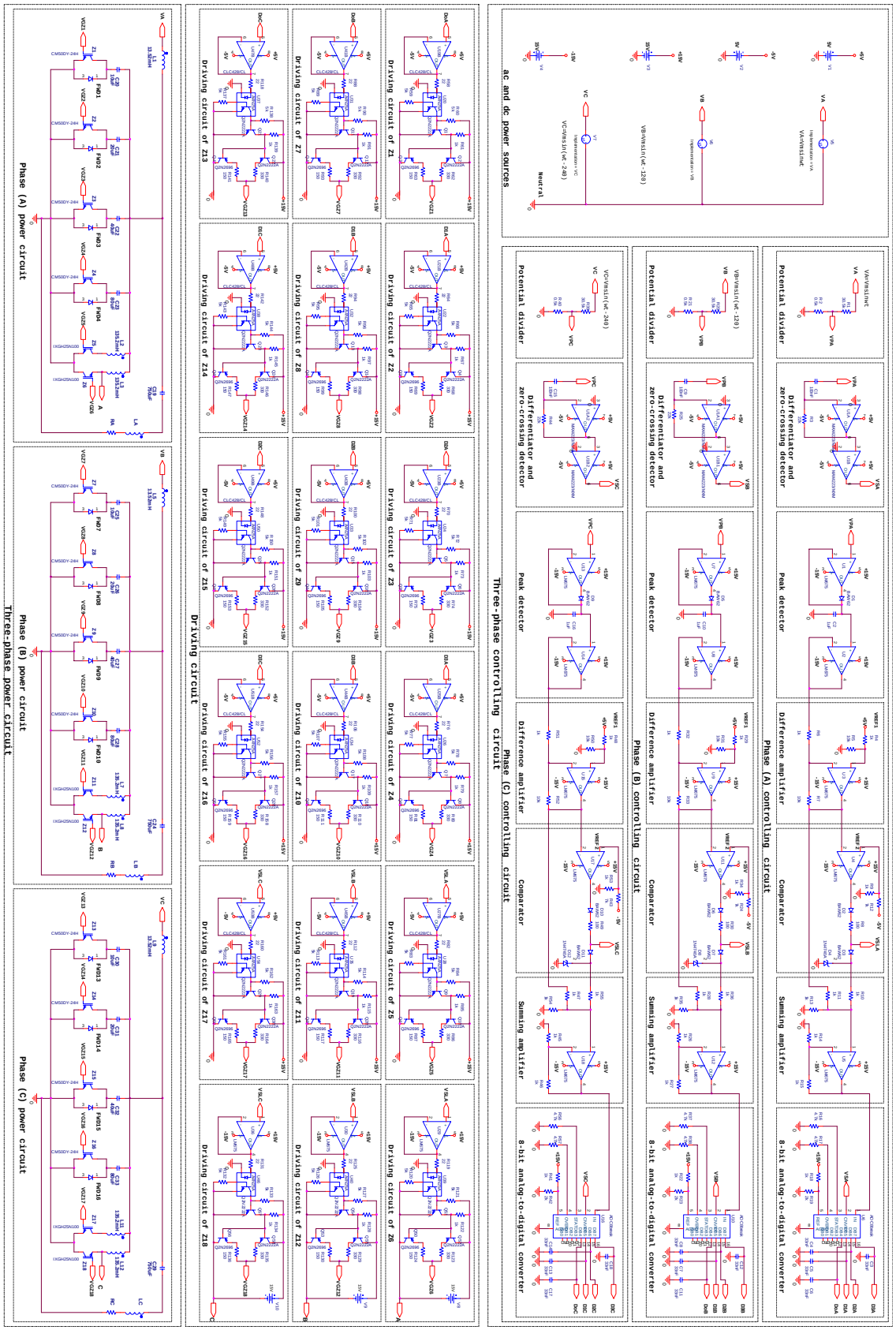


Fig. 7 The circuit diagram of the adopted three-phase regulator.

4. 1 The Three-phase controlling circuit

This circuit is designed such that each load phase voltage is maintained at 220V rms, even though the input phase voltages are varying within the range of (176V to 264V) rms at a frequency of 50Hz.The three-phase controlling circuit includes three identical circuits. The controlling circuit of phase (A) is shown in **Fig. 8**. The three-phase supply is note assumed to be balanced within the above range of variations. Phase (A) input voltage V_A is stepped down to $0.0161V_A$ through the potential divider and then peak detected to $\sqrt{2}\times0.0161V_A=0.0227V_A$ through the peak detector. Since each input phase voltage is expected to be within the above range, the peak detector output will possibly vary from 4V to 6V. Note that the peak value of V_A will be bounded within the range of (248.8V to 373.2V). The peak detector output is subtracted from the reference voltage V_{REF1} and then multiplied by 2 through the difference amplifier to produce a dc voltage of $2(5-0.0227V_A)$. When V_A= 220V rms, $0.0227V_A$ will be equal to 5V which represents V_{REF1}. The output of the difference amplifier will be positive when V_A<220V rms and negative when V_A>220V rms. Whenever the output of the difference amplifier is more positive than V_{REF2}= -0.625V, the output of the comparator is zero, and the output of the summing amplifier will equal the output of the difference amplifier. When the output of the difference amplifier is less negative than V_{REF2}, the comparator output will be 10V and the summing amplifier output will be $(20-0.0454V_A)$. The output of the summing amplifier will be zero when V_A rises to $1.2V_L$=264V rms. Note that V_L is 220V rms which represents the rated load phase voltage. When V_A varies from 220V to 176V rms, the analogue input of the 8-bit analog-to- digital converter varies from zero to 10V leading to produce stepping capacitive susceptance varying from zero to 15ωC with a capacitive susceptance step of ωC. When V_A varies from 220V to 264V rms, the analogue input of the 8-bit analog-to- digital converter varies from 10V to zero leading to the addition of a constant inductive susceptance of -15ωC and a stepping capacitive susceptance varying from 15ωC to zero with a capacitive susceptance step of -ωC. Consequently, the net inductive susceptance will vary in stepping manner from zero to -15ωC. 8-bit analog-to-digital converters were used in the design process for sake of obtaining more accuracy.

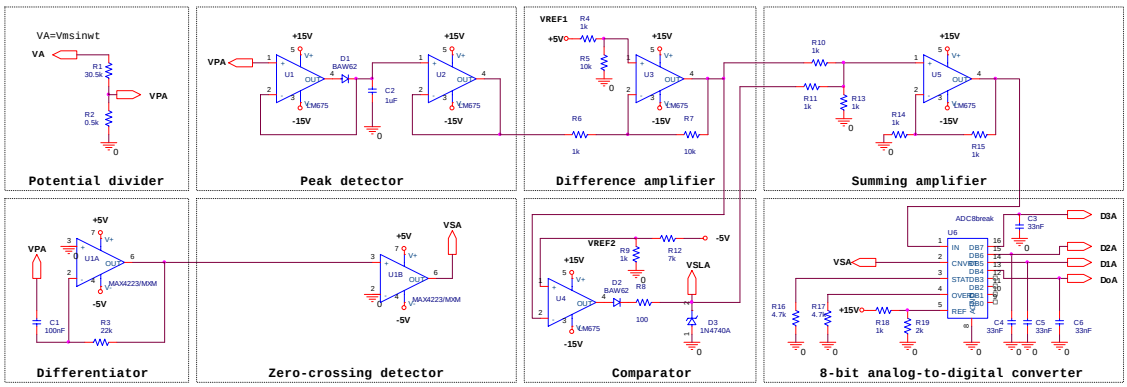


Fig. 8 Phase (A) controlling circuit.

4. 2 The driving circuit

Each switching device requires a proper driving circuit designed in such a manner that the switching on and the switching off are guaranteed at the specified times with minimum switching energy losses. The switching device employed for the capacitor bank is the Insulated-Gate Bipolar Transistor (IGBT) of the type CM50D-y-24H which has the following maximum ratings: collector current I_C=50A, collector to emitter voltage V_{CE}=1200V, gate to emitter voltage V_{GE}= ±20V, junction temperature T_C=150C^o, and collector power dissipation P_C=400W. The energy switching losses for the employed switching devices are almost negligible, since the switching processes occur only when there are changes in phase voltages. **Fig. 9** shows the driving circuit of the switching device Z1. Here RON offers the path for charging the IGBT input capacitance C_i=14.75nF through the transistor Q2, ROFF represents the discharging path for C_i through the transistor Q3.

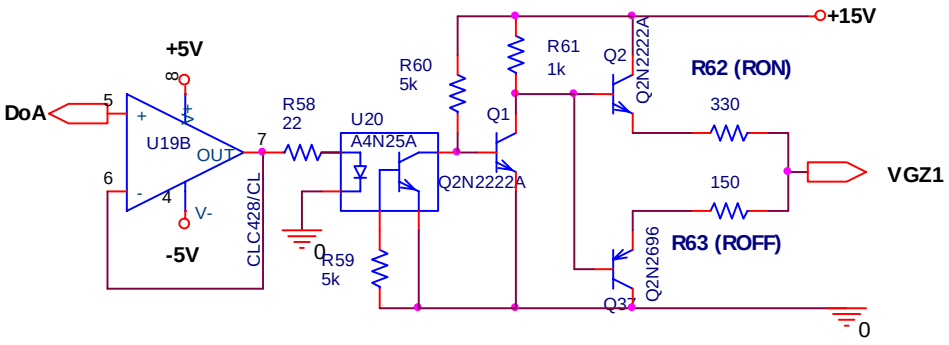


Fig. 9 The driving circuit of the switching device Z1.

4. 3 The three-phase power circuit

The power circuit of the adopted three-phase regulator consists of three identical circuits. The power circuit of phase (A) is shown in **Fig.10**. The switched inductor here is represented by two inductors L2 and L3 in order to avoid the dc term associates the switching instant which is lasting for several cycles of the input phase voltage waveform.

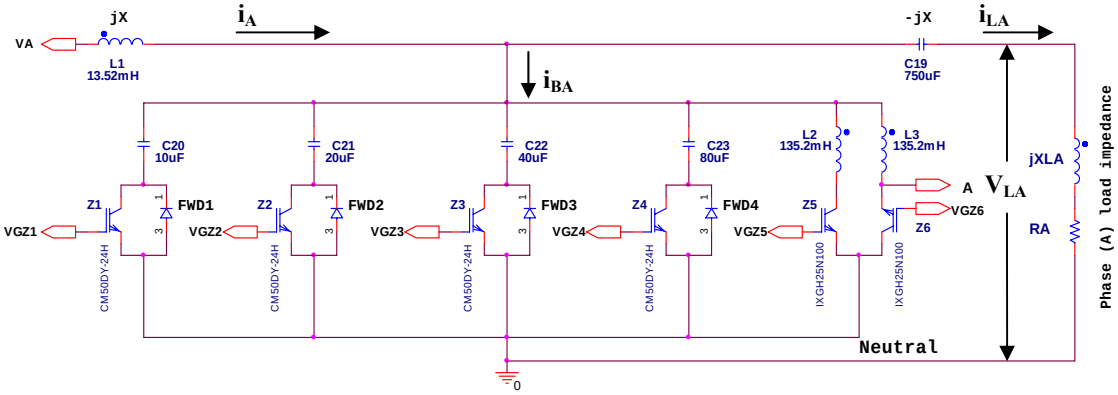


Fig. 10 Phase (A) power circuit.

During the switching process, the inductor current will be $(1-\cos\omega t)V_m/\omega L$ if the inductor is switched on at $\omega t=0$ from an input voltage of $V_m \sin\omega t$ and will be $-(1+\cos\omega t)V_m/\omega L$ if the inductor is switched on at $\omega t=\pi$ (Rashid 2002). L2 will be switched on at $\omega t=0$ and hence its current i_{L2} will contain the dc term $(V_m/\omega L)$, while L3 will be switched on at $\omega t=\pi$ and its current i_{L3} will contain the dc term $(-V_m/\omega L)$. The total current of both inductors i_{LT} will be $-2(V_m/\omega L)\cos\omega t$ which is shown in **Fig. 11** as a pure inductive current. Consequently, the inductance of L2 or L3 must be 2L in order that the total inductive current will be $-(V_m/\omega L)\cos\omega t$. Note that L is the inductance shown in **Fig. 3**. Z1, Z2, Z3, and Z4 are insulated-gate bipolar transistors IGBTs provided with fast recovery freewheel diodes FWD1 FWD2, FWD3, and FWD4. These freewheel diodes are responsible for delivering the negative half-cycles of the capacitive currents, While the IGBTs are responsible for the positive half-cycles. When a certain IGBT is OFF, its corresponding freewheel diode will charge its own capacitor to $-V_m$ and then stop conducting for a long time. Z1, Z2, Z3, and Z4 are specified in **Section (4. 2)**. Z5 and Z6 are IGBTs of the type IXGH25N100, which have the following maximum ratings: collector current I_C=50A, collector to emitter voltage V_{CE}=1000V, gate to emitter voltage V_{GE}= ±20V, junction temperature T_C=150C^o, and collector power dissipation P_C=200W. These IGBTs are not equipped with freewheel diodes.

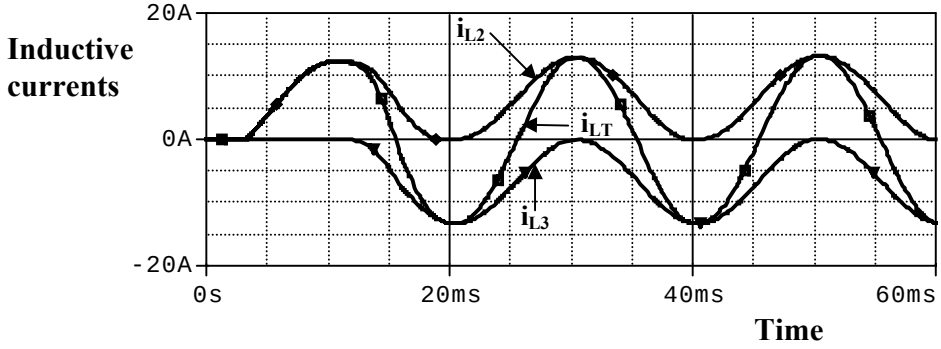


Fig. 11 The production of a pure sinusoidal inductive current.

5. Simulation results

The system was tested on PSpice at a frequency of 50Hz and a temperature of 27C^o. The rated phase voltage is 220V rms (311V peak) and the rated impedance absolute value is 20.25Ω.The first group of tests were made on a balanced three-phase voltage which had dropped to 80% of its rated value. The results of that test were taken after five cycles of phase (A) input voltage (i.e. after 100msec) and are shown in **Fig. 12**. Note that load phase voltages V_{LA}, V_{LB}, and V_{LC} are raised to 220V rms and driven in phase with the corresponding input phase voltages V_A, V_B, and V_C for both resistive and inductive loads. In addition, the input phase currents i_A, i_B, and i_C in **Fig. 12b**, are slightly leading the input voltages V_A, V_B, and V_C respectively. Since the input phase currents in **Fig. 12** are leading their corresponding phase voltages, an amount of leading reactive power is added to the power system network causing a proportional rise in the system terminal three-phase voltage.

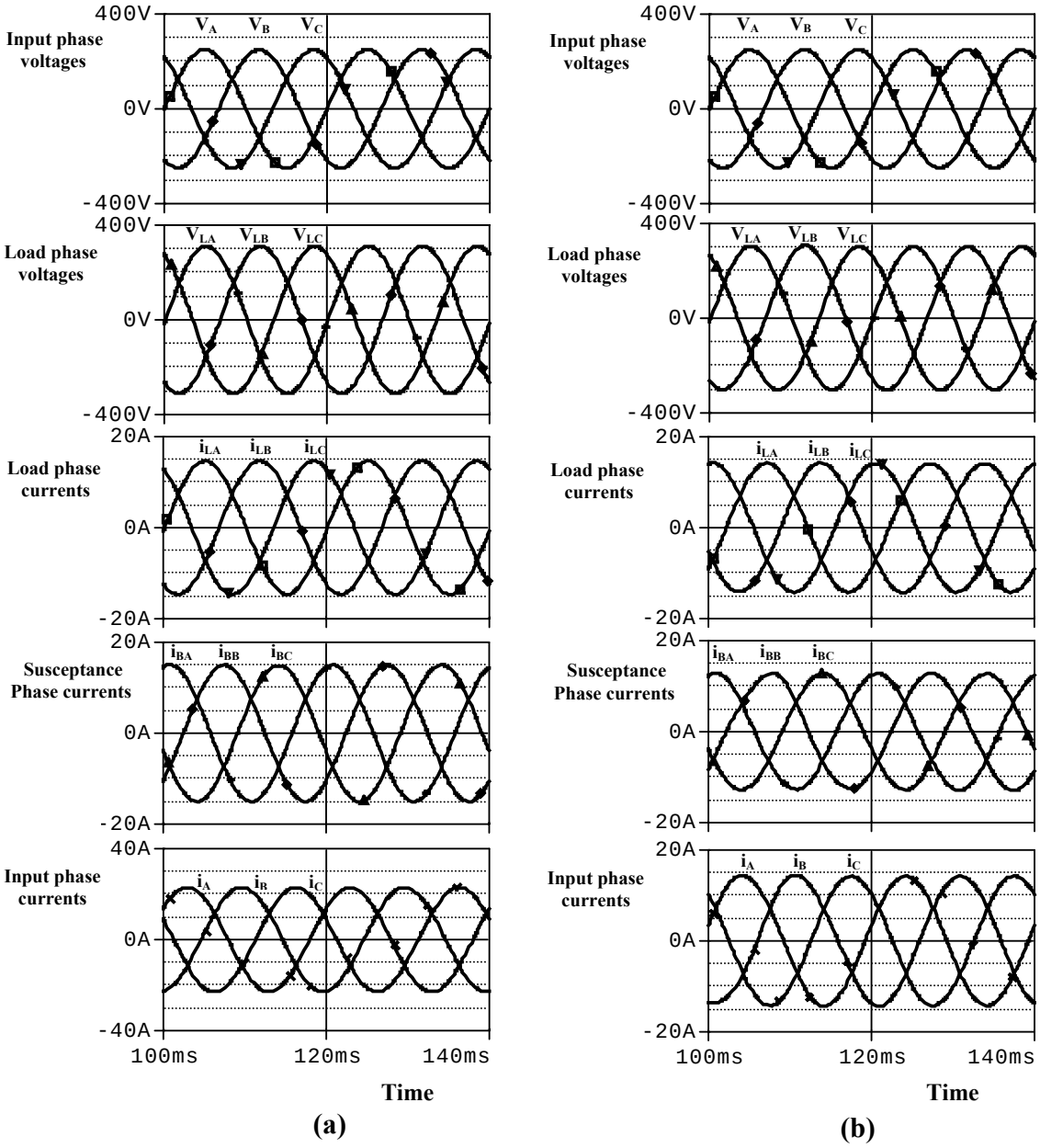


Fig. 12 Regulator voltage and current waveforms during a drop in each input phase voltage of 20% of its rated value at full-load operation with balanced three-phase (a) pure resistive load, (b) inductive load running at 0.8 power factor.

The second group of tests were done for a balanced voltage rise in the three-phase voltage of 20% of its rated value for both balanced resistive and inductive full loads as shown in **Fig. 13**. Here load phase voltages V_{LA}, V_{LB}, and V_{LC} are lowered to 220V rms and driven in phase with the corresponding input phase voltages V_A, V_B, and V_C for both resistive and inductive loads. Also the input phase currents i_A, i_B, and i_C are lagging behind their corresponding input phase voltages causing an absorption of reactive power

from the power system network which in turn leads to a proportional reduction in the system terminal three-phase voltage. During full load operation, the inductive load phase currents are almost equal to the input phase currents for both voltage rise and voltage drop in the input phase voltages.

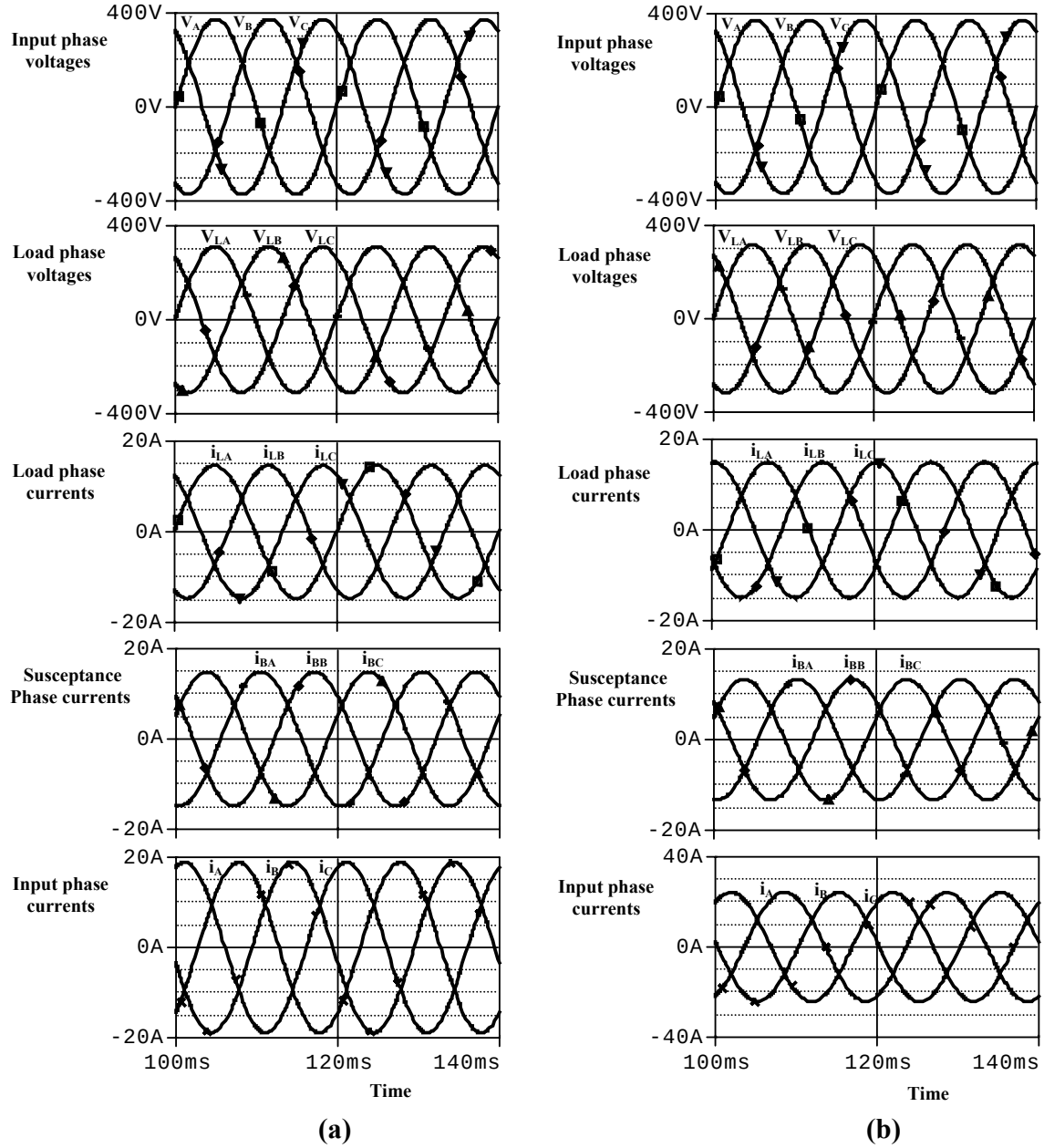


Fig. 13 Regulator voltage and current waveforms during a rise in each input phase voltage of 20% of its rated value at full-load operation with balanced three-phase (a) pure resistive load, (b) inductive load running at 0.8 power factor.

The final tests were made on two different unbalanced three-phase voltages shown in **Fig. 14.** For both cases, the load phase voltages are brought to their rated values and driven in phase with their corresponding input voltages even though the load impedances were randomly specified. **Fig. 14a** states that the input phase voltage V_B is within its rated level and hence phase (b) susceptance current i_{BB} is zero. Also in **Fig. 14a, V_A** suffered voltage drop and V_C suffered voltage rise. Consequently their corresponding susceptance phase currents i_{BA}, and i_{BC} will be pure capacitive and pure inductive currents respectively. The same mechanism will be applied for **Fig. 14b** waveforms**.**

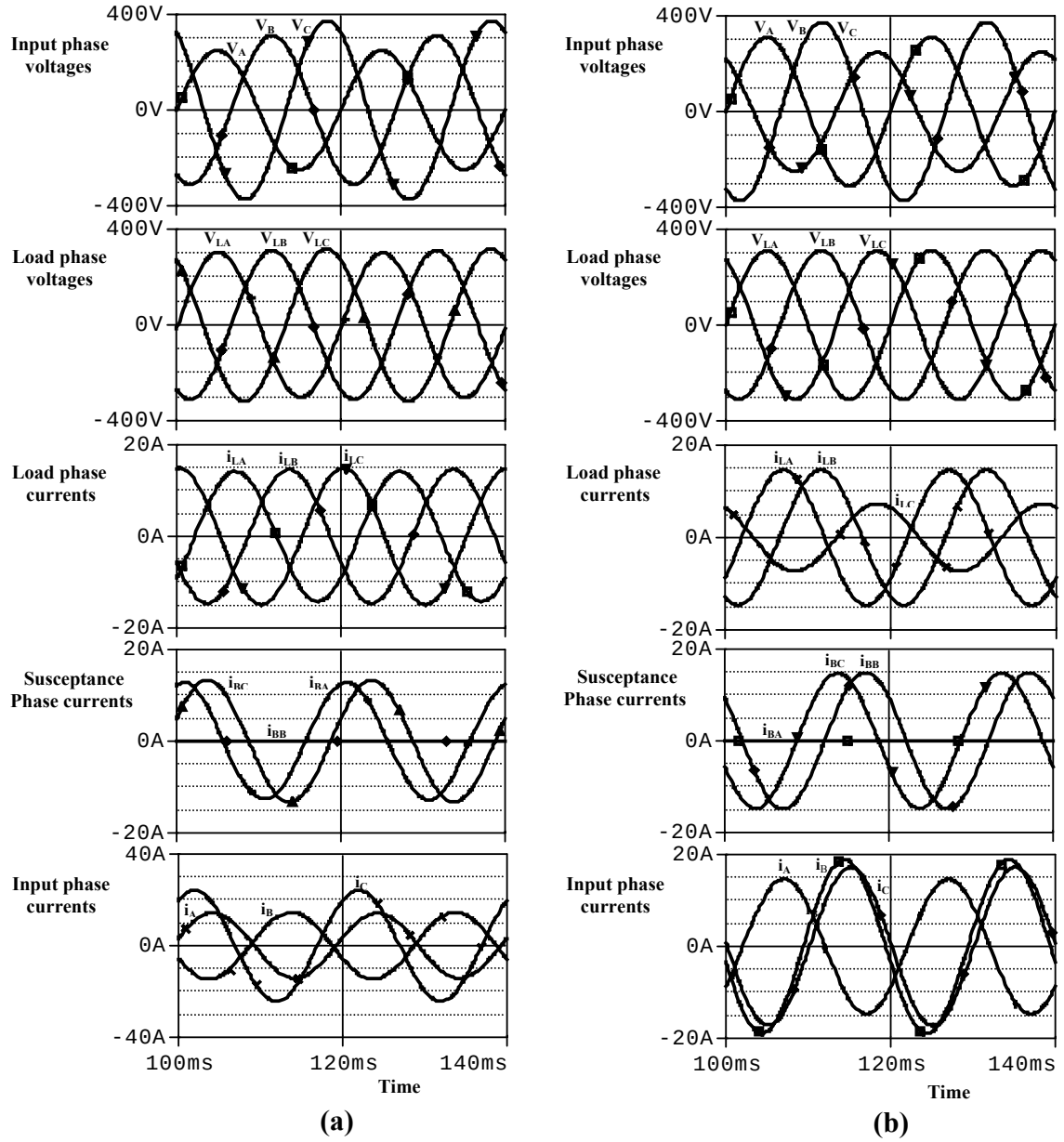


Fig. 14 Voltage and current waveforms during random changes in input phase voltages when the regulator was (a) fully loaded by balanced 0.8 power factor inductive impedance, (b) randomly loaded.

6. Conclusion

This regulator has a wide field of applications because its design is characterized by high flexibility for extending to wide ranges of power and voltage. Consequently, it can find applications for heavy industrial loads besides light load applications. Since the conventional loads are almost inductive, this regulator exhibits power factor correction during the compensations of the power system voltage drops and this is clearly indicated in **Fig. 12**. The regulator treats each input phase voltage individually and drives the phase load voltage to its rated value. Results have demonstrated that only the changes in the input phase voltages are required for producing the phase susceptance currents capable of bringing the load phase voltages to their rated values. In addition, results have ensured that load currents will have no effects on regulator operation if they are within their rated values. Load phase voltages were successfully compensated and balanced in all tests without any significant generation of harmonics. Load balancing identity of this regulator, improves the performance of three-phase loads amongst voltage fluctuations.

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