Design of a 31-Level Single-Phase Voltage-source Inverter Producing almost Sinusoidal Voltage Waveform

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Abstract

In this paper a single-phase voltage-source inverter of 31 non-zero levels is designed. These levels follow a sinusoidal path and are constructed by using only five dc voltage sources instead of thirty-one as traditionally employed in multilevel technology of voltage-source inverters. Consequently, the total numbers of switching devices and electronic circuitries are largely reduced. The output voltage of this inverter has sinusoidal form and is almost free from harmonics associating conventional types of inverters. No type of conventional Pulse-Width-Modulation is introduced here and the technique is applicable for both resistive and inductive loads. The complete system was designed and implemented on Pspice.

الخلاصة

في هذا العمل تم تصميم عاكس للفولتية يقوم بتوليد فولتية أحادية الطور ذات واحد وثلاثين مستوى غير صفري متساوية التباعد وتتبع مسارا جيبي الشكل. هذه المستويات تم تشكيلها باستخدام خمسة مصادر لفولتية التيار المباشر بدلا من إحدى وتلاثين مصدرا كما هو مستخدم في التقنيات التقليدية التي تتبنى إنتاج الفولتيات المتعددة المستويات. وصاحب هذا التخفيض في عدد المصادر تخفيضا كبير في عدد الأجهزة المفتاحية والدوائر الالكترونية اللازمة لها. فولتية الإخراج لهذا العاكس ذات شكل جيبي وخالي تقريبا من التوافقيات الملازمة للعاكسات التقليدية. لم يستخدم في هذا النظام أي نوع من أنواع تعديل عرض النبضة التقليدي. وهذه التقنية ملائمة للأحمال الحثية والأحمال ذات المقاومة النقية. تم إجراء التصميم واختباره باستخدام البرنامج ألتشبيهي (PSpice).

1. Introduction

Inverters are the most efficient means of dc to ac power conversion and have an important role in variable ac drive industries. They witnessed an excessive hierarchy of developments throughout the recent years. The multilevel technology is one of those developments where the shaping of the output voltage waveforms of inverters has been assigned as the main target of this technology. Efforts were exerted to construct sinusoidal voltage waveforms at the output of voltage source inverters. The space-vector techniques had adopted the achievement of output voltages constituting sinusoidal envelopes with their average values (Teodorescu et al 2002, Mailah et al 2009). Those techniques had employed intelligent gate drive to design microcontrollers for triggering the switching devices of voltage-source inverters. Researchers, who are interested in multilevel techniques, aspire to approach sinusoidal voltage waveforms at the output of voltage-source inverters (Tolbert et al 1999, Mekhilef and Masaoud 2006, Pandian and Reddy 2008), but this requires large numbers of dc voltage sources and switching devices, in addition to the complex circuitry associating them. Since the number of voltage levels is restricted by the complexity of the inverter circuitry, designers tend to accept limited levels and treat each level by a certain Pulse-Width-Modulation technique besides a proper harmonics elimination technique (Manguelle and Rufer 2001, Kumar et al 2008). Here in the adopted design, thirty-one non-zero levels were constructed for each half cycle of the single-phase voltage at the output of the voltage-source inverter using only five separate dc voltage sources and no type of conventional Pulse-Width-Modulation was employed.

2. Construction of a 31-nonzero level unidirectional voltage supply

The system employs five dc voltage sources to construct thirty-one nonzero voltage levels. **Fig. 1** states the technique that achieves the above strategy. The multilevel voltage Vmlt is simply the resultant of the activated voltages of the five dc sources, which are controlled by the logic of the five most significant digits of an 8-bit analog-to-digital converter (8-bit ADC). The dc voltage sources are weighted according to the weights of digits controlling them.

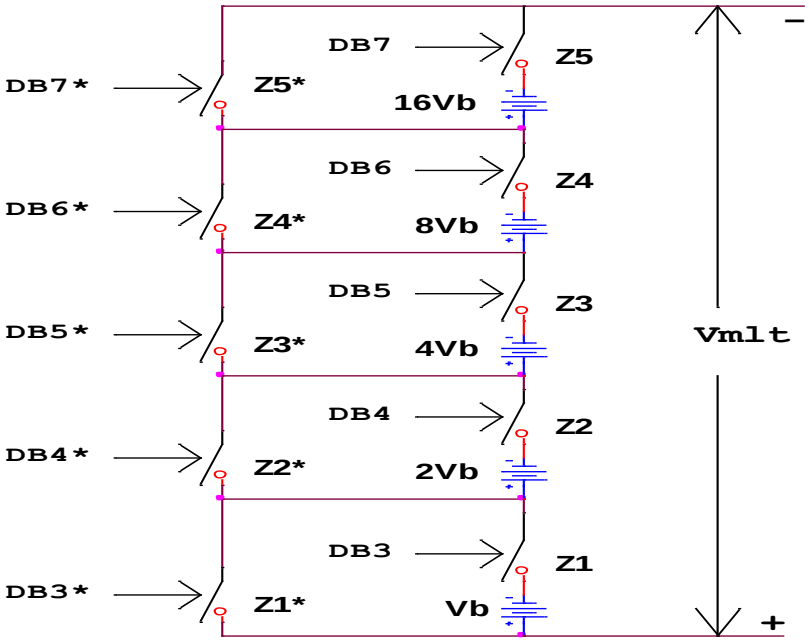


Fig . 1 The multilevel voltage production circuit.

If the input of the ADC is the positive half cycle of a sinusoidal voltage signal having amplitude of 10 volts and frequency of 50Hz, then the voltage Vmlt will exhibit the voltage waveform shown in **Fig. 2**. Here, V_b represents the voltage step, which is simply the difference between two adjacent levels and is denoted by the base voltage. The five dc voltage sources will be V_b, $2V_b$, $4V_b$, $8V_b$, and $16V_b$ according to the weights of the five most significant digits controlling their switches Z1, Z2, Z3, Z4, and Z5. For example, DB3, DB4, DB5, DB6, and DB7 control the voltage sources V_b, $2V_b$, $4V_b$, $8V_b$, and $16V_b$ respectively, while the switches Z1*, Z2*, Z3*, Z4*, and Z5* are controlled by the complements DB3*, DB4*, DB5*, DB6*, and DB7* respectively. Consequently, when a certain Z switch is in OFF state, then the corresponding Z* switch will be in ON state and vice versa. **Table (1)** shows the truth table of the controlling logic, the status of the switching devices, and the corresponding values of Vmlt.

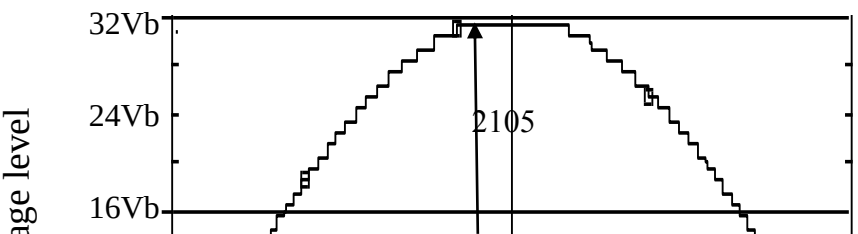
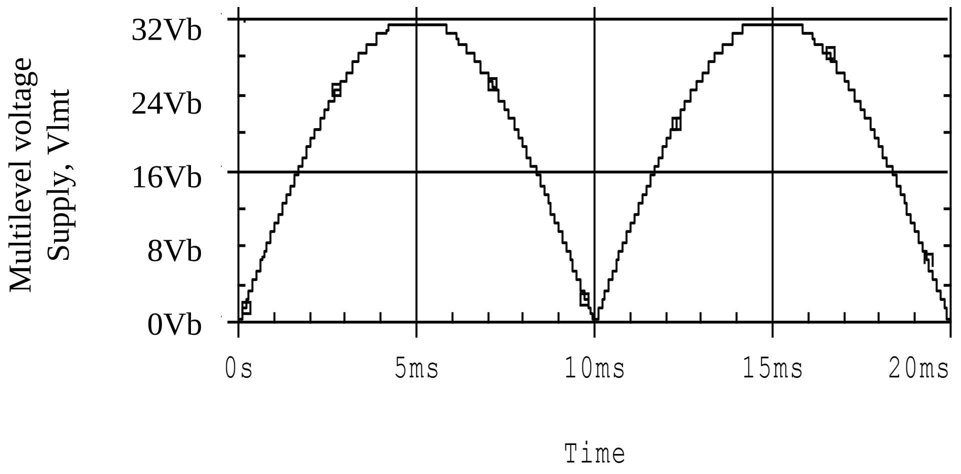


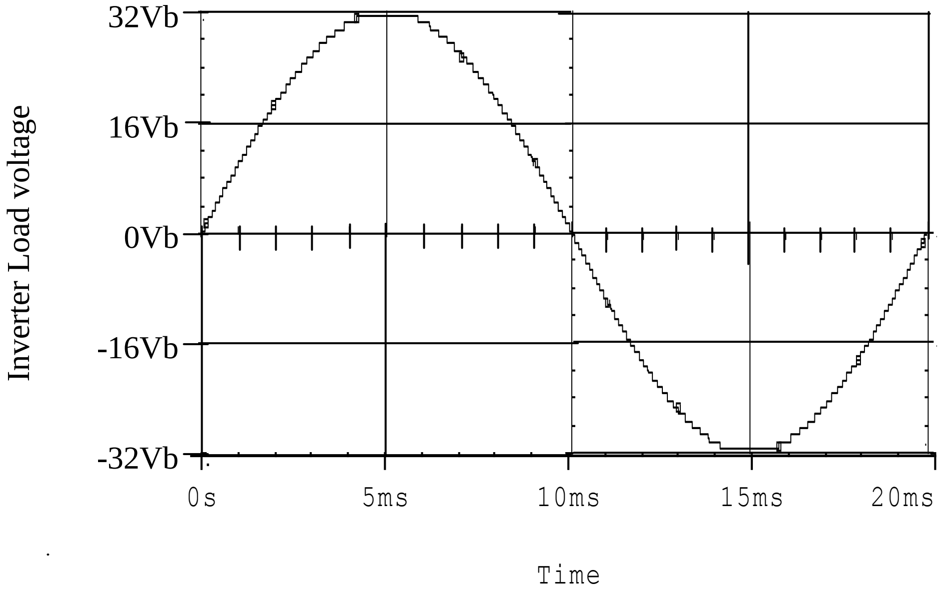
Table (1) The truth table of the 31- level voltage supply.

DB7	DB6	DB5	DB4	DB3	Z5	Z4	Z3	Z2	Z1	Z5*	Z4*	Z3*	Z2*	Z1*	Vmlt
0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	0
0	0	0	0	1	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	Vb
0	0	0	1	0	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	2Vb
0	0	0	1	1	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	3Vb
0	0	1	0	0	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON	4Vb
0	0	1	0	1	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF	5Vb
0	0	1	1	0	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	6Vb
0	0	1	1	1	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	7Vb
0	1	0	0	0	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	8Vb
0	1	0	0	1	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	9Vb
0	1	0	1	0	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	10Vb
0	1	0	1	1	OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	11Vb
0	1	1	0	0	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	12Vb
0	1	1	0	1	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	13Vb
0	1	1	1	0	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	14Vb
0	1	1	1	1	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	15Vb
1	0	0	0	0	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	16Vb
1	0	0	0	1	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	17Vb
1	0	0	1	0	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	18Vb
1	0	0	1	1	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	19Vb
1	0	1	0	0	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	20Vb
1	0	1	0	1	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	21Vb
1	0	1	1	0	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	22Vb
1	0	1	1	1	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	23Vb
1	1	0	0	0	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	24Vb
1	1	0	0	1	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	25Vb
1	1	0	1	0	ON	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	26Vb
1	1	0	1	1	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	27Vb
1	1	1	0	0	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	28Vb
1	1	1	0	1	ON	ON	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	29Vb
1	1	1	1	0	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	30Vb
1	1	1	1	1	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	31Vb

When a precision full-wave rectifier for a 10V peak sinusoidal waveform, produces the analogue input to the 8-bit ADC, the path of thirty-one voltage levels of Vmlt will follow the shape of the positive halves of a sinusoidal voltage waveform as shown in **Fig .3a**. The multilevel voltage Vmlt will actually be the main supply of a somewhat modified single-phase voltage-source inverter bridge to form the sought inverter. Since the conventional single-phase voltage-source inverter is characterized by reversing the current and voltage through the load, its output will attain sinusoidal form as shown **in Fig.3b**.



(a)



(b)

Fig. 3 (a) The 31-level voltage supply, (b) the inverter load voltage.

2.1 The fundamental component of the inverter load voltage

A seven nonzero-level voltage is suggested here for simplifying the derivation of the fundamental component of any N-level load voltage. **Fig. 4** shows this voltage. Vmsinωt is the voltage desired to be generated. It is a sinusoidal voltage of amplitude Vm and angular frequency ω. V_L is the multilevel voltage, which is built of seven-nonzero levels. Note that the total number of voltage levels (including the zero level) is eight and the voltage step (V_b) is Vm/8. If a multilevel voltage of N-nonzero levels is required to be constructed, then the voltage step will be {Vm/(N+1)}. Substituting for ωt by θ, the height of the shaded rectangular in **Fig. 4** is given by:

$$kV_b = Vm\sin\theta_k \quad \text{..} \quad (1)$$

Where K is the number of a certain voltage level and varies from 0 to N. θ_k is equated to be:

$$\theta_k = \sin^{-1}\left(kV_b / Vm\right)$$

$$= \sin^{-1}\left(k/(N+1)\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Where $Vm/V_b = N+1$.

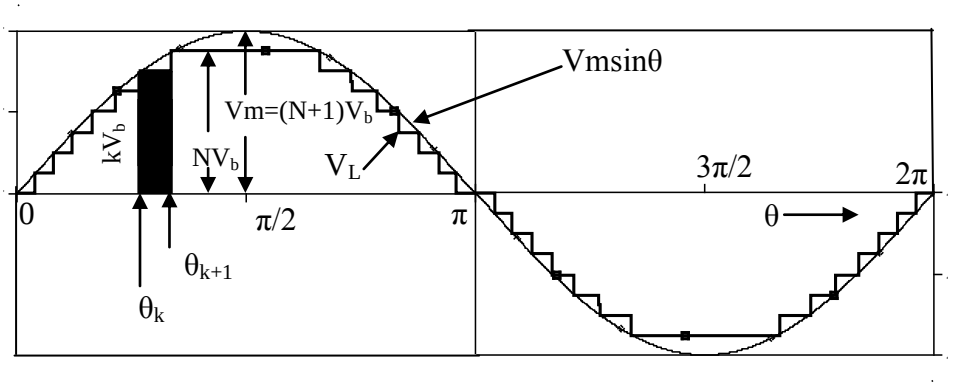


Fig . 4 Seven-level voltage construction.

The fundamental component a_1 of the load voltage V_L is determined by using Fourier series as follows (Wylie 1975):

$$a_1 = \left(1/\pi\right)\int_0^{2\pi} V_L \sin(\theta)\,d\theta$$

$$= \sum_{k=0}^{k=N}\left(4/\pi\right)\int_{\theta_k}^{\theta_{k+1}} kV_b \sin(\theta)\,d\theta$$

$$= \sum_{k=0}^{k=N}\left(4kV_b/\pi\right)\left(\cos(\theta_k) - \cos(\theta_{k+1})\right)$$

$$= \sum_{k=0}^{k=N}\left(4kV_b/\pi\right)\left(\sqrt{1-\left(k/(N+1)\right)^2} - \sqrt{1-\left((k+1)/(N+1)\right)^2}\right) \quad \ldots\ldots (3)$$

The ratio (a_1/Vm) is computed for values of N from 3 to 255 and then plotted against these values as shown in **Fig. 5**. It is obvious that this ratio tends to unity while N is increasing. **Table (2)** shows the numeric variations of a_1/Vm and V_b against N when Vm is 320 volts. It is recommended here to mention that the operating frequency of V_L is unlimited, but it is obviously understood to be within the usual ac drive ranges.

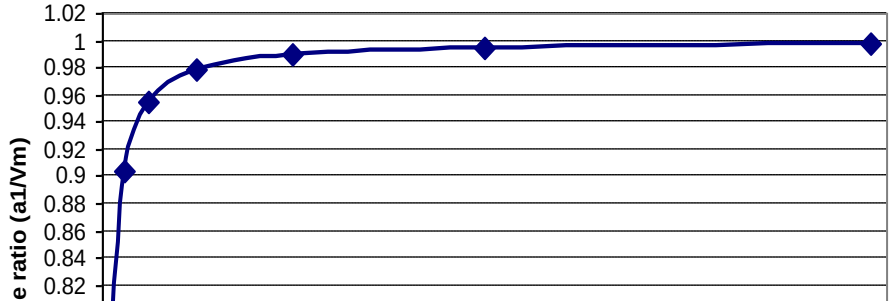
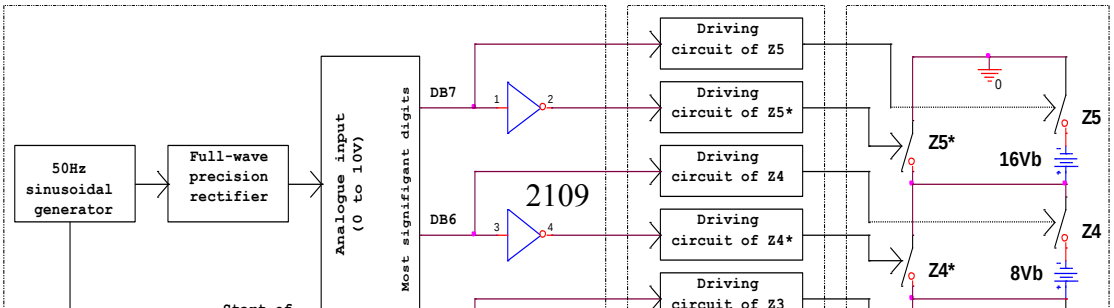


Table (2) The variations of load voltage fundamental with nonzero levels.

Number of nonzero voltage levels, N	Fundamental component, a_1 (volts)	Base voltage, V_b (volts)	Percentage (a_1/Vm) (100%)
3	254.34	80	79.17
7	289.41	40	90.44
15	305.55	20	95.484
31	313.13	10	97.85
63	316.74	5	98.98
127	318.49	2.5	99.52
255	319.34	1.25	99.79

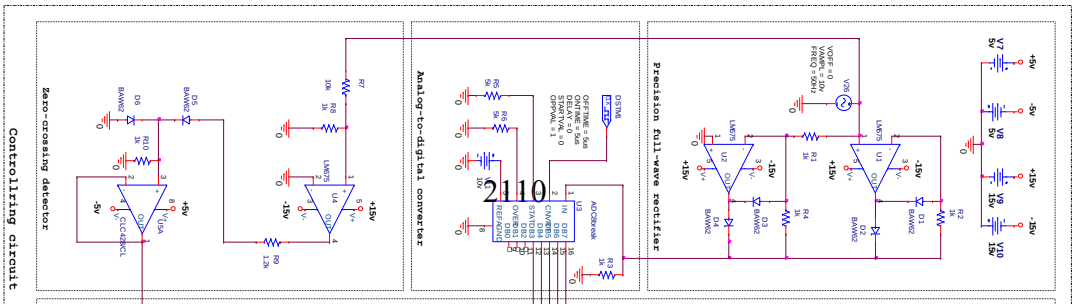
3. The proposed inverter design scheme

The schematic diagram of the proposed inverter is shown in **Fig. 6**. The 50Hz signal having amplitude of 10V is full-wave rectified and fed to the 8-bit ADC, which converts it to digital at a frequency of 100 KHz. The five most significant digits of the 8-bit ADC are employed with their complements to control the Z and the Z* switching devices which are insulated-gate-transistors driven by proper electrically insulated electronic circuits. The positive and negative half cycles of the load voltage are demonstrated according the voltage-source bridge performance constructed by S1, S2, S3, and S4.



The 31-non-zero levels inverter circuit diagram:

Fig. 7 shows the whole system circuit diagram which is designed on PSpice. All the datasheets of the electronic parts were taken into account during the design process. It is recommended here to concern the circuits of this diagram separately for the sake of stating the system performance. The circuit diagram follows the schematic diagram shown in **Fig. 7** and hence there are three main circuits to be identified here.



4. 1 The controlling circuit

This circuit is shown in **Fig. 8**. It consists of three sub circuits, which are the precision full-wave rectifier, analog-to-digital converter, and the zero-crossing

detector. The full-wave rectifier precision circuit is a standard one and its function is the full-wave rectification of a sinusoidal voltage having amplitude of 10 volts and frequency of 50 Hz (Malmstadt et al 1981). The rectified voltage, which is varying between 0 and 10 volts, is exerted at the input of the 8-bit ADC. The ADC outputs DB7, DB6, DB5, DB4, DB3, DB2, DB1, and DBo will be all high when its input is 10 volts and all low at zero input. Only the most five significant digits DB7, DB6, DB5, DB4, and DB3 are used. Consequently, the above action reveals the behavior of a 5-bit ADC. The zero-crossing detector prepares the square waveforms required for operating a conventional voltage-source inverter. **Fig. 9** shows the signal waveforms of this circuit.

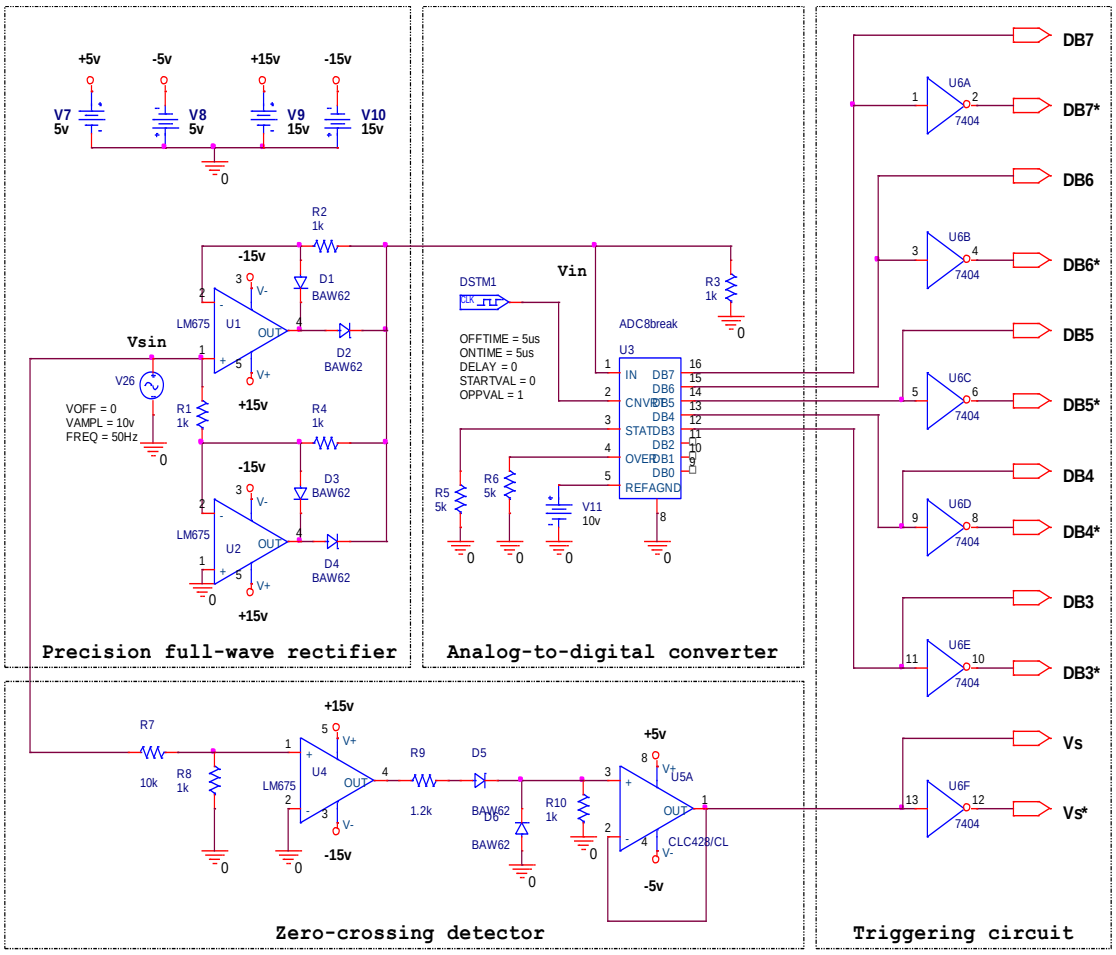
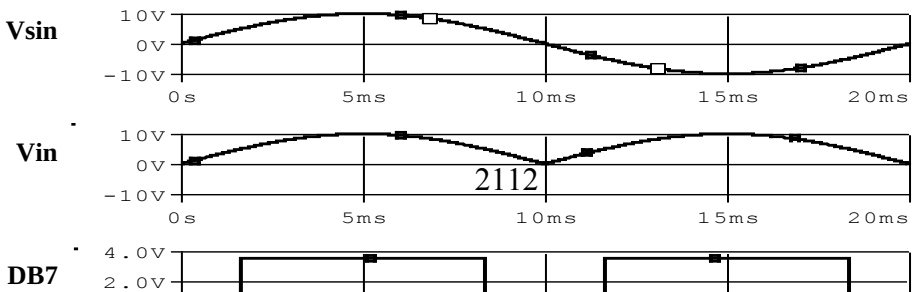


Fig. 8 The controlling circuit

The latter circuit is the triggering circuit, which consists of six digital inverters. The outputs of them are the logic compliments of DB7, DB6, DB5, DB4, DB3, and Vs, which will be used later for triggering the power circuit switching devices. The circuit diagram of **Fig .8** states the function of this sub circuit.



4. 2 The driving circuit

The diving circuit includes fourteen identical sub circuits as obviously indicated in the whole circuit diagram shown in **Fig. 7**. Each sub circuit is designed according to the datasheet of the switching device to be driven which is an insulated-gate bipolar transistor (IGBT) of the type IRGBC40F. **Fig. 10** shows the driving circuit of the IGBT Z5. The resistance R_{ON} is chosen to be greater than R_{OFF} for forbidding the instantaneous commutation of toggling IGBT's by completing the turning off for a

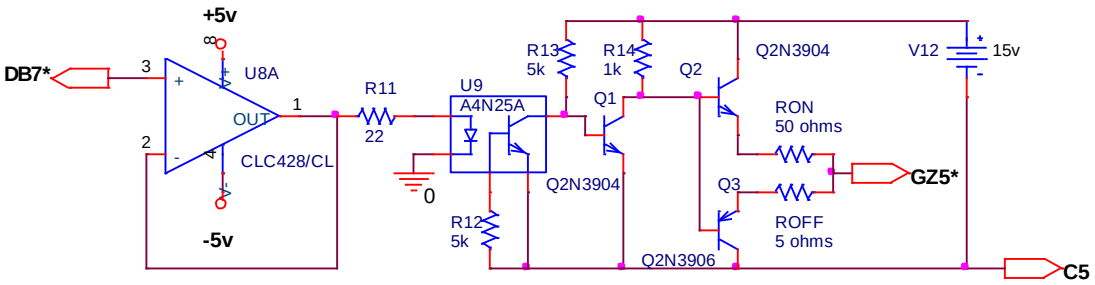


Fig. 10 The driving circuit of the IGBT Z*5.

certain IGBT before the conduction of the other (Rashid 2001). For example the IGBT's Z1 and Z1* are two toggling switching devices and hence when one of them

is required to be ON the other must be OFF and vice versa. **Fig. 11** shows the gate currents of Z1 (iGZ1) and Z1* (iGZ1*). Note that iGZ1 is the IGBT input capacitance (C_{GS}) charging current flowing through R_{ON}, while iGZ1* is the discharging current flowing through R_{OFF}. When this capacitance charges to more than 12 volts, the device will be fully conducting and when its voltage falls to below 5 volts; this means that the device is completely OFF. Note that the charging process takes more time than discharging process.

4. 3 The power circuit

This circuit is shown in **Fig. 12** and it consists of two sub circuits. The first sub circuit is the most important one, since it builds the multilevel voltage shown in **Fig. 1**. The switching devices of this sub circuit are functioning according to **Table (1)**. It is required for this inverter to supply a sinusoidal voltage of amplitude of 320 volts and frequency of 50Hz. The base voltage V_b is calculated to be 10 volts and hence the maximum voltage level ($31V_b$) shown in **Fig. 3b**, will exhibits 310 volts in the neighborhood of t=5msec. The second sub circuit is a modified single-phase voltage source bridge (Skvarenina 2001). It consists of three parts; a smoothing circuit, a freewheeling circuit, and an inverter bridge assigned by S1, S2, S3, and S4.

The inverter bridge is conventional and is operating according to the sequence that S1 and S2 are ON when the status of the controlling signal Vs, is high and S3 and S4 are ON when the controlling signal Vs* is high. Note that Vs* is the logic complement of Vs.

The smoothing circuit consists of a capacitor C1 in series with the parallel combination of L1 and DSM. C1 helps to smooth the load voltage envelope while L1 serves as a current limiter and DSM serves as a freewheeling path for the energy stored in L1 (Millman and Halkias 1983).

The freewheeling circuit is a series combination of C2, the two anti-parallel freewheeling diodes FWD1 and FWD2, and the parallel combination of C4 and L2. When the load is inductive, this circuit is operated manually by using the switch SL. During resistive loads, SL is open. The value of the capacitor C2 is decided by the value of the reactive load current. L2 is a current limiter and C4 is a limiter of rapid voltage changes. The IGBT used is characterized by V_{CEmax} (Maximum collector to emitter voltage) =600V, I_{Cmax} (Maximum collector current) =49A, P_{CMAX} (Maximum collector dissipation) =160W, V_{CEsat} (Collector to emitter saturation voltage) <1.8V, and C_{GS} (input capacitance) =1.04nF. The voltage source V6 is employed to

compensate for the total voltage drop across the conducting IGBTs (seven IGBTs are conducting at the same time). Ten volts for this source is sufficient for compensation.

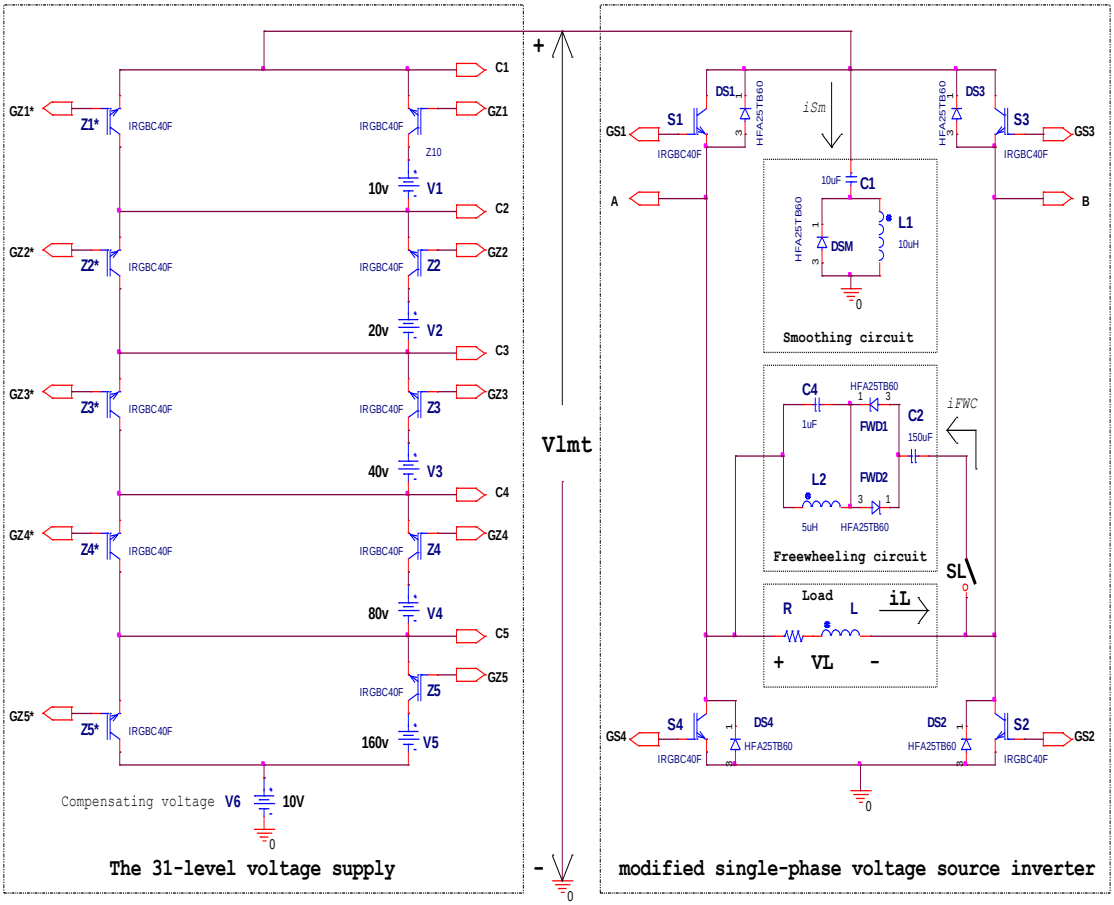
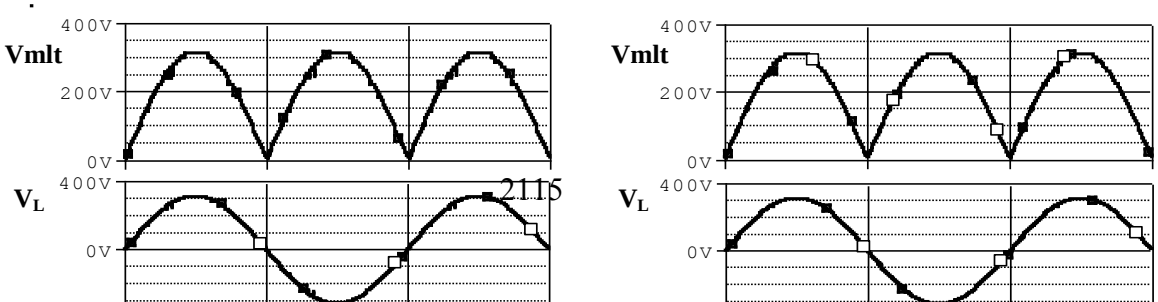


Fig. 12 The power circuit of the 31-level single-phase voltage source inverter.

5. Results

The system was tested on PSpice at 27C^{o} for both resistive and inductive loads. For resistive loads, the inverter operating frequency was 50Hz, the rms load voltage required was 220 volts, and the rated load impedance was 10 ohms. For inductive load loads, the inverter frequency was changed in the range of 25Hz to 75Hz and the load voltage was changed in such a manner that a constant voltage to frequency ratio was guaranteed during ac drive applications, which required constant torques. The load voltage value can be controlled by adjusting the value of the base voltage V_b within voltage sources V1, V2, V3, V4, and V5. This action can be achieved automatically, if controlled rectifiers produce these five sources. **Fig. 13** shows the voltage and current waveforms associating two different resistive loads. **Fig. 14** shows two inductive loads operating at nominal frequency (50Hz) and rated voltage (220 volts rms) with a power factor of 0.8. The first load is running at full load while the second is running at half-full load.



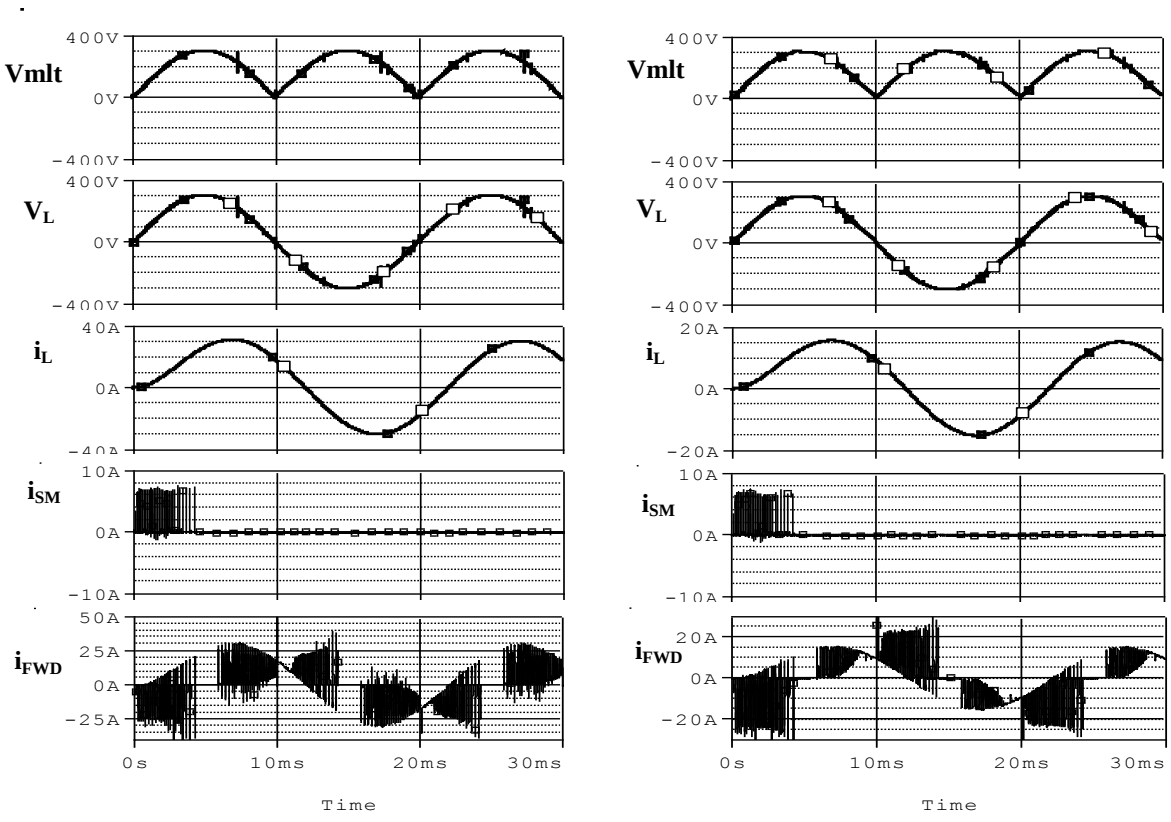


Fig. 14 Voltage and current waveforms for a 0.8 p.f inductive load, (a) Z_L=10Ω, (b) Z_L=20Ω.

Fig. 15 shows voltage and current waveforms for a load running at 25Hz, 50Hz, and 75Hz. For the three load conditions, voltage to frequency ratio was kept constant by changing V_b for each case. V_b was adjusted to 5 volts, when the required frequency f was 25Hz and adjusted to 15 volts when f was 75Hz. The load impedance $\mathbf{Z_L}$ in that

case had **R**=8.5Ω and **L**=16.8mH. Consequently, $\mathbf{Z_L}$ was calculated to be 8.9Ω for f=25Hz, 10Ω for f=50Hz, and 11.61Ω for f=75Hz. The power factor values for those cases were 0.955, 0.85, and 0.732.

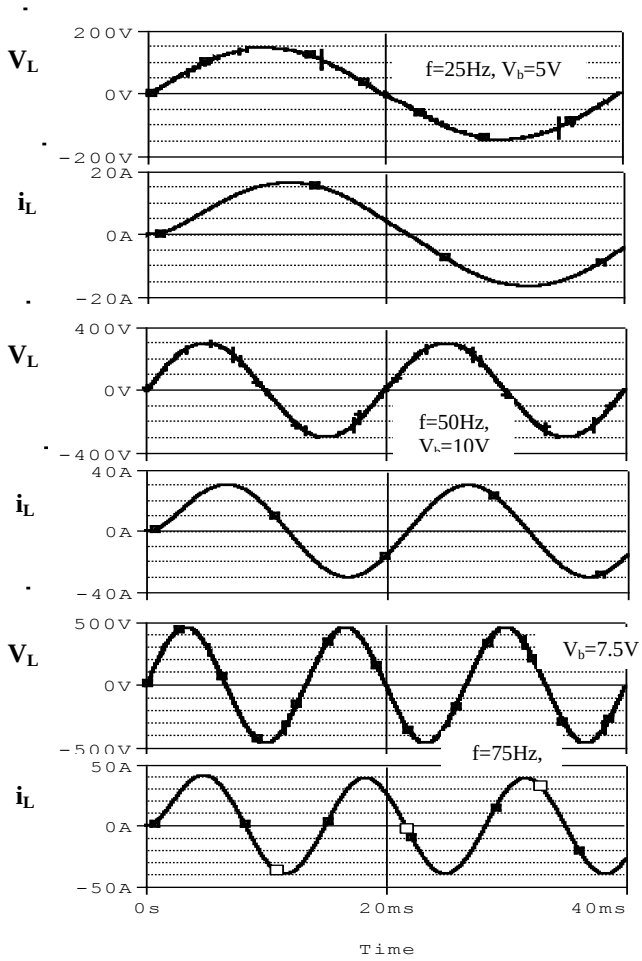


Fig. 15 Voltage and current waveforms for a load having R=8.5Ω and L=16.8mH under variable ac drive operation.

The voltage to frequency ratio was calculated and plotted against frequency as shown in **Fig. 16**. It is obvious that this ratio is almost constant.

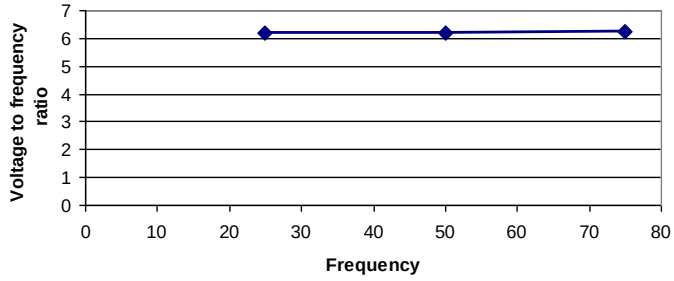


Fig. 16 voltage to frequency rato under ac drive operation.

5. Conclusion

The new approach has succeeded in the production of a sinusoidal voltage waveform for high power purposes. In addition, it offers the possibility of the extension to high voltage dc transmission technology where pure sine waves are the

utmost aspirations. The three-phase configuration is possible and it will certainly be the future work of this approach. The fundamental component of the produced voltage in **Table (2)** leads to the conclusion that, the best numbers of nonzero levels are rounded by 15 and 31, which are revealing a good compromise between quality and economical cost. Since the fundamental component of the 31-level voltage is very close to the desired voltage amplitude, the harmonic components associating the generated voltage are almost negligible. The current waveforms for both resistive and inductive loads reflect sinusoidal behaviors.

This technique is characterized by the reduction of numbers of power voltage sources and switching devices. The number of voltage sources is reduced to $\log_2 (N+1)$ instead of N. Consequently, the number of switching devices will be reduced in the same manner. It is obvious that this technique is economically utilized.

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