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Full Length Research Paper

Design of an almost continuously controlled three-phase static VAR compensator for power factor correction purposes

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In this paper, a three-phase four-wire automatic power factor correction system is designed and tested. This system employs three-phase Wye-connected thyristor switched-capacitor banks to generate a controllable static VAR. Each capacitor bank is constructed of five binary weighted thyristor switched-capacitors. This arrangement leads to a capacitor bank capable of generating stepping reactive power having thirty one equidistant non-zero levels. The controlling circuit of each capacitor bank is designed such that maximum absolute deviation from linear response is 1/62 of its rating. Each capacitor is controlled by a single thyristor shunted by a reverse diode. The system is capable of correcting lagging power factor up to unity or adjusting it according to user desire. Each capacitor is connected to a series reactor for protecting the solid state combination from inrush current occurring at the first instant of compensator plug in to power system network. The proposed system is characterized by negligible no load operating losses, no generation of harmonics, energy saving, and reduction of transmission losses. The system is designed and implemented on PSpice which is a computer program very close in performance to real hardware and broadly adopted by manufacturing companies.

Key words: Capacitor bank, power factor correction, power quality, static VAR.

INTRODUCTION

Power factor improvement leads to a big reduction of apparent power drawn from the ac source which in turn saves energy and minimizes the transmission losses (Mehrdad, 2005; Dai et al., 2007; Lupin et al., 2007). It generally employs means that control reactive power in power system network (Gyugy et al., 1978). The process is usually denoted by reactive power compensation which is a productive technology employed for improving power systems performance. This technology serves customers and power system networks. Power quality is an insisting challenge in ac power systems, whereas reactive power compensation techniques offer striking solutions on the route of its achievement. Reactive power control solves or attenuates many power system problems such as poor voltage regulation, line currents unbalance, poor power factor, and reduced efficiency. There are so many techniques approaching reactive power control, but the static VAR compensators are the most reliable ones, since they present high flexibility in design methodology and exhibit reasonable response amongst fast varying environments (Miller, 1982). Static VAR compensators are either series or shunt compensators. Series compensators deal with modification of distribution or transmission parameters of the ac system, while shunt compensators decide the load equivalent impedance (Miller, 1982; Teleke et al., 2008). Both types of compensators can be used to control the reactive power for power factor correction purposes in ac power systems.

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Synchronous condensers and manually switched capacitors or inductors can be used for power factor correction purposes, but. static VAR compensators using thyristor switched- capacitors and thyristor controlled reactors are superior to them, since they are characterized by fast response and high design flexibility (Teleke et al., 2008). Fixed capacitor-thyristor controlled reactor (FC-TCR) compensators are widely used for power factor correction purposes. They offer the feasibility of continuous reactive power control, but they exhibit full load operating losses at relaxation time, since the TCR is operating at its full capacity in order to absorb the reactive power generated by the fixed capacitor (Chen et al., 1999). In addition they release large amounts of harmonic current components which increase transmission losses and disturb the power system network voltage profile (Best and La Parra, 1996). The TCR is a source of harmonics, where the third harmonic for instance is about 13% of the TCR rating (Chen et al., 1999). This reveals the need for harmonics filters which add more complexity and more operating and transmission losses (Lee and Wu, 2000). Static VAR compensators using switched-capacitor banks offer stepping responses in reactive power generation mode and their losses are proportional to the reactive power demands (Nandi et al., 1997). FC-TCR and switched capacitor banks static VAR compensators are usually referred to as conventional static VAR compensators which are basically characterized by the employment of naturally commutated solid-state switching devices having high voltage and current ratings.

Employment of converters with an appropriate pulse width modulation control technique, permits the implementation of static VAR compensators capable of generating or absorbing reactive power with fast time response (Walker, 1986; Stahlkopf and Wilhelm, 1997). The recent developments in power electronics devices offer high amount of flexibility in static VAR compensators design for power factor correction and voltage control purposes. The new generations of these devices are characterized by fast responses, wide frequency spectrums, wide safe operating areas, low switching losses, low ON and OFF times, and easy commutation (Rashid, 2001; Bimal, 2006). Basing on the above facts and the recent analytical computations, Flexible AC Transmission Systems (FACTS) appear as a new concept in power transmission systems (Idris et al., 2010).

These new technologies make it easy to present static VAR compensators having fast response and capable of increasing the amount of apparent power through a transmission line in the neighborhood of its thermal capacity, without exceeding its stability limits. These new technologies are limited to low voltage applications, since they are employing fast solid-state switching devices having relatively low voltage and current ratings (Rashid, 2001; Bimal, 2006).

Here in this paper, a reliable switched-capacitors technique is adopted for three-phase automatic power factor correction purposes. The technique is based on designing a switched-capacitor bank exhibiting almost linear response versus reactive power demand. This technique solves the linearity problem of static VAR generation and offers the feasibility of operation at high voltage and current ratings, since it employs solid state switching devices having high ratings. In addition, the proposed technique is harmonic free, thus no harmonic filters are required.

THE CAPACITOR BANK CONFIGURATION

The proposed capacitor bank is composed of five binary weighted capacitors as shown in Figure 1a. This configuration offers 31 non-zero levels of possible capacitive reactive current as shown in Figure 1b. Each capacitor is controlled by a single thyristor shunted by a reverse diode. The thyristor handles the positive half cycle of the capacitor current and the diode deals with the negative half cycle. Reactors L_{S1} to L_{S5} are current limiters.

THE PROPOSED SINGLE-PHASE SYSTEM

The single-phase power factor correction system block diagram is shown in Figure 2. The capacitor bank triggering circuit is excited by two signals. The first signal is Ki_L, where K is the attenuation factor of the current transformer (C.T) circuitry and i_L is the instantaneous load current. The second signal is K^*v, where K* is the attenuation factor of the voltage transformer (V.T) circuitry and v is the instantaneous phase voltage.

The load voltage and current can be given by:

$$v = V_m \sin \omega t \quad (1)$$

$$i_L = I_m \sin(\omega t - \varphi) \quad (2)$$

Where V_m is the load voltage amplitude in volts, I_m is the load current amplitude in amperes, φ is load current power factor angle in radians, and t is time in seconds. The first zero-crossing detector in Figure 2 converts K^*v to a rectangular waveform V_1 which is then differentiated and half-wave rectified by the first RC differentiator/rectifier, forming V_2. The latter is a train of pulses used to trigger the sample and hold circuit at $\omega t = n\pi$, where n is a positive odd integer. The analogue differentiator converts K^*v to the analogue signal V_3

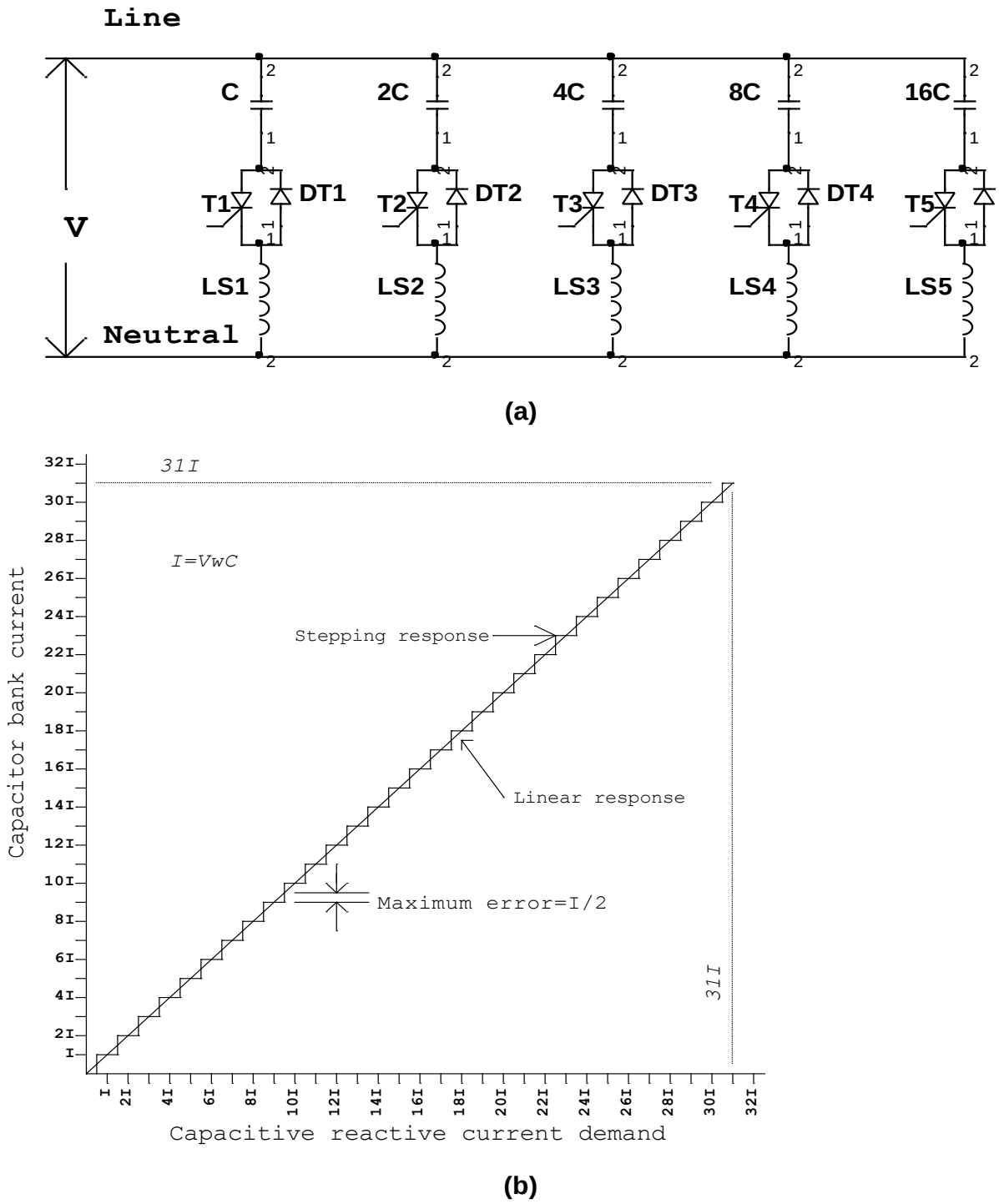

Figure 1. Capacitor bank, (a) configuration, (b) expected reactive current response.

which is then zero-crossing detected, forming the waveform V_4. The latter is processed similar to V1, forming V_5. These waveforms are shown in Figure 3.

The current signal Ki_L is sampled by the sample and hold circuit at $\omega t = n\pi$, where n is a positive odd integer, yielding an analogue signal proportional directly to the

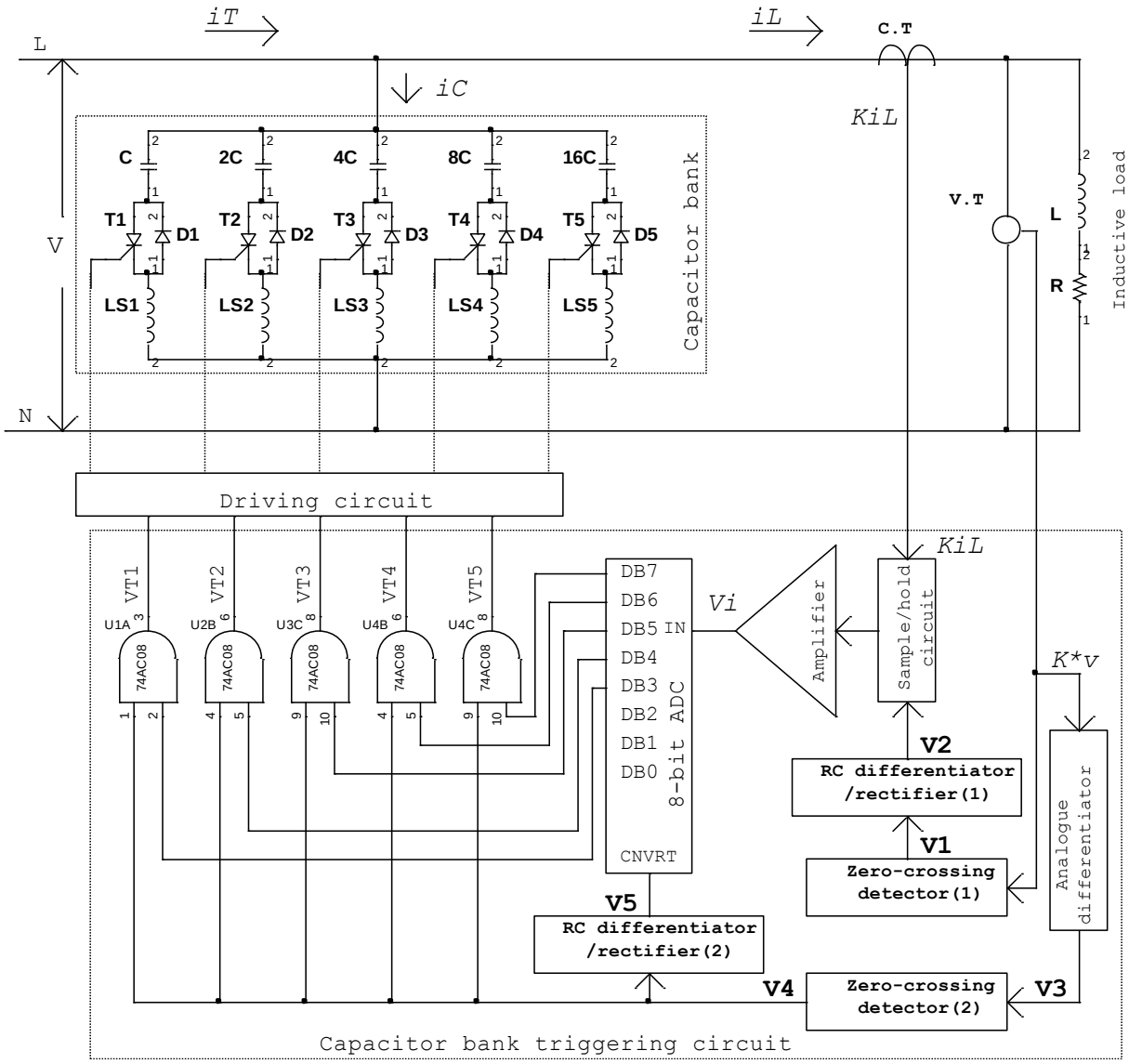

Figure 2. The proposed single phase power factor correction system block diagram.

reactive current component of the load current as follows:

$$\left(Ki_L = KI_m \sin(\omega t - \varphi)\right)^{\omega t = n\pi} = KI_m \sin\varphi \qquad (3)$$

The latter signal is amplified and clamped upward by 0.15625 volts producing the analogue voltage V_i which is proportional to the reactive current demand. V_i is the analogue input of the 8-bit analogue-to-digital converter (8-bit ADC). For unity power factor correction and at full compensator rating, V_i will have a magnitude of 10 volts. The 8-bit ADC starts conversion at ωt = (2n-1)π/2, where n is a positive odd integer. The five most significant digits (*DB7*, *DB6*, *DB5*, *DB4*, and *DB3*) of the 8-bit ADC are employed for controlling the capacitor bank switching devices (T_5, T_4, T_3, T_2, and T_1) respectively. The instantaneous capacitor bank current i_C is determined by the logic status of the 8-bit ADC as follows:

$$i_C = V_m \omega C\left[\frac{16}{5}DB7 + \frac{8}{5}DB6 + \frac{4}{5}DB5 + \frac{2}{5}DB4 + \frac{1}{5}DB3\right] \qquad (4)$$

Where, C is the basic capacitance of the capacitor bank. For *DB7*, *DB6*, *DB5*, *DB4*, and *DB3*, logic zero refers to zero volts, while logic one refers to +5 volts. Note that when V_i is zero, all the digital outputs of the 8-bit ADC are

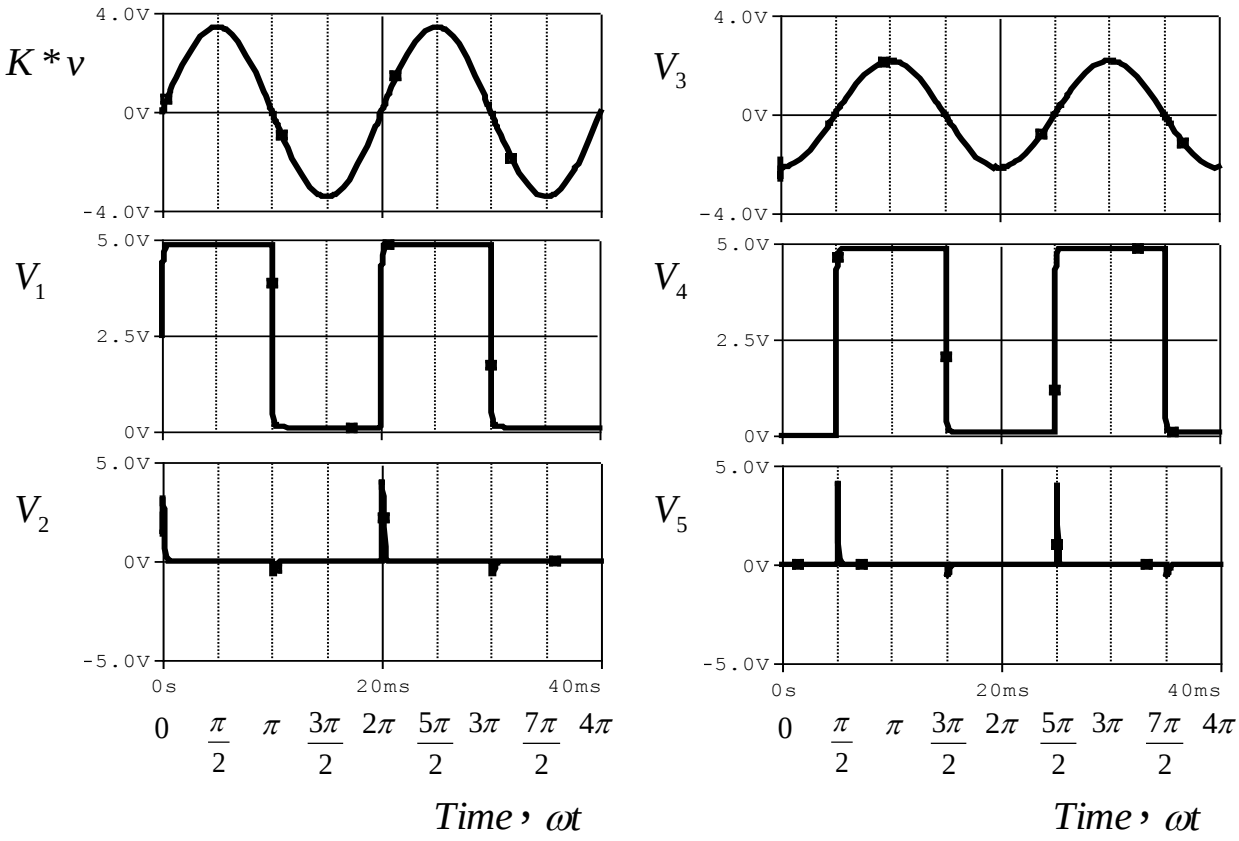

Figure 3. The single-phase basic voltage waveforms.

logic zero. When V_i is 10 volts, all the digital outputs are logic one.

Table 1 shows the capacitor bank switching status as V_i varies from zero to 10 volts. The driving circuit includes five sub-circuits; each one of them deals with one of the thyristor (T_1 to T_5). Choosing appropriate switching instants will protect the switching devices from inrush currents. The appropriate switching of thyristor occurs at ωt = (2n+1)π/2, where n is a positive odd integer. At these instants *dv/dt* is zero and each of the capacitors (C, 2C, 4C, 8C, and 16C) is charged to $-V_m$ through its corresponding diode and limiting reactor. Note that when this compensator is started, each of the above capacitors charges through its individual diode and limiting reactor to $-V_m$. No inrush current will associate the charging and switching mechanisms.

THE PROPOSED THREE-PHASE POWER FACTOR CORRECTION SYSTEM

The power circuit of three-phase power factor correction system is shown in Figure 4. It is simply composed of three identical capacitor banks connected in star form. i_{CA}, i_{CB}, and i_{CC} are the instantaneous compensator phase currents, while v_A, v_B, and v_C are the power system instantaneous phase voltages. The three phase instantaneous load currents are i_{LA}, i_{LB}, and i_{LC}, while the three phase instantaneous line currents are i_A, i_B, and i_C. Each capacitor bank will respond according to Figure 1b.

The block diagram of the proposed three-phase four-wire power factor correction system is shown in Figure 5. It comprises three identical voltage transformers and three identical current transformers. Here are three identical triggering circuits; each one of them deals with a single capacitor bank. Phase A triggering circuit is excited by the analogue signals Ki_{LA} and K^*v_A, phase B triggering circuit is excited by the analogue signals Ki_{LB} and K^*v_B, and phase C triggering circuit is excited by the analogue signals Ki_{LC} and K^*v_C. If the compensator is operated by a balanced three-phase supply, then the controlling signals can be given by

$$K^* v_A = K^* V_m \sin \omega t \qquad (5)$$

Table 1. The capacitor bank status as V_i varies from 0 to 10 V.

Vi (Volts)	C_1 Status	C_2 Status	C_3 Status	C_4 Status	C_5 Status
0	OFF	OFF	OFF	OFF	OFF
0.3125	ON	OFF	OFF	OFF	OFF
0.625	OFF	ON	OFF	OFF	OFF
0.9375	ON	ON	OFF	OFF	OFF
1.25	OFF	OFF	ON	OFF	OFF
1.5625	ON	OFF	ON	OFF	OFF
1.875	OFF	ON	ON	OFF	OFF
2.1875	ON	ON	ON	OFF	OFF
2.5	OFF	OFF	OFF	ON	OFF
2.8125	ON	OFF	OFF	ON	OFF
3.125	OFF	ON	OFF	ON	OFF
3.4375	ON	ON	OFF	ON	OFF
3.75	OFF	OFF	ON	ON	OFF
4.0625	ON	OFF	ON	ON	OFF
4.375	OFF	ON	ON	ON	OFF
4.6875	ON	ON	ON	ON	OFF
5	OFF	OFF	OFF	OFF	ON
5.3125	ON	OFF	OFF	OFF	ON
5.625	OFF	ON	OFF	OFF	ON
5.9375	ON	ON	OFF	OFF	ON
6.25	OFF	OFF	ON	OFF	ON
6.5625	ON	OFF	ON	OFF	ON
6.875	OFF	ON	ON	OFF	ON
7.1875	ON	ON	ON	OFF	ON
7.5	OFF	OFF	OFF	ON	ON
7.8125	ON	OFF	OFF	ON	ON
8.125	OFF	ON	OFF	ON	ON
8.4375	ON	ON	OFF	ON	ON
8.75	OFF	OFF	ON	ON	ON
9.0625	ON	OFF	ON	ON	ON
9.375	OFF	ON	ON	ON	ON
9.6875	ON	ON	ON	ON	ON

$$K^{*}v_B = K^{*}V_m \sin\left(\omega t - 2\pi/3\right) \quad (6)$$

$$K^{*}v_C = K^{*}V_m \sin\left(\omega t - 4\pi/3\right) \quad (7)$$

$$Ki_{LA} = KI_{mLA} \sin\left(\omega t - \phi_A\right) \quad (8)$$

$$Ki_{LB} = KI_{mLB} \sin\left(\omega t - 2\pi/3 - \phi_B\right) \quad (9)$$

$$Ki_{LC} = KI_{mLC} \sin\left(\omega t - 4\pi/3 - \phi_C\right) \quad (10)$$

Where I_{mLA}, I_{mLB}, and I_{mLC} are the load phase currents amplitudes, while φ_A, φ_B, and φ_C are their power factor angles. These three-phase controlling signals are processed in the same manner adopted in the single phase power factor correction system. The capacitor bank of each phase will respond according to the criterion of Table 1.

SYSTEMS CIRCUITS DESIGN

The single-phase and three-phase automatic power factor correction systems are designed and implemented using the computer program PSpice. Datasheets of electronic parts and aiding literatures are considered during design process (Rashid, 2001; Bimal, 2006).

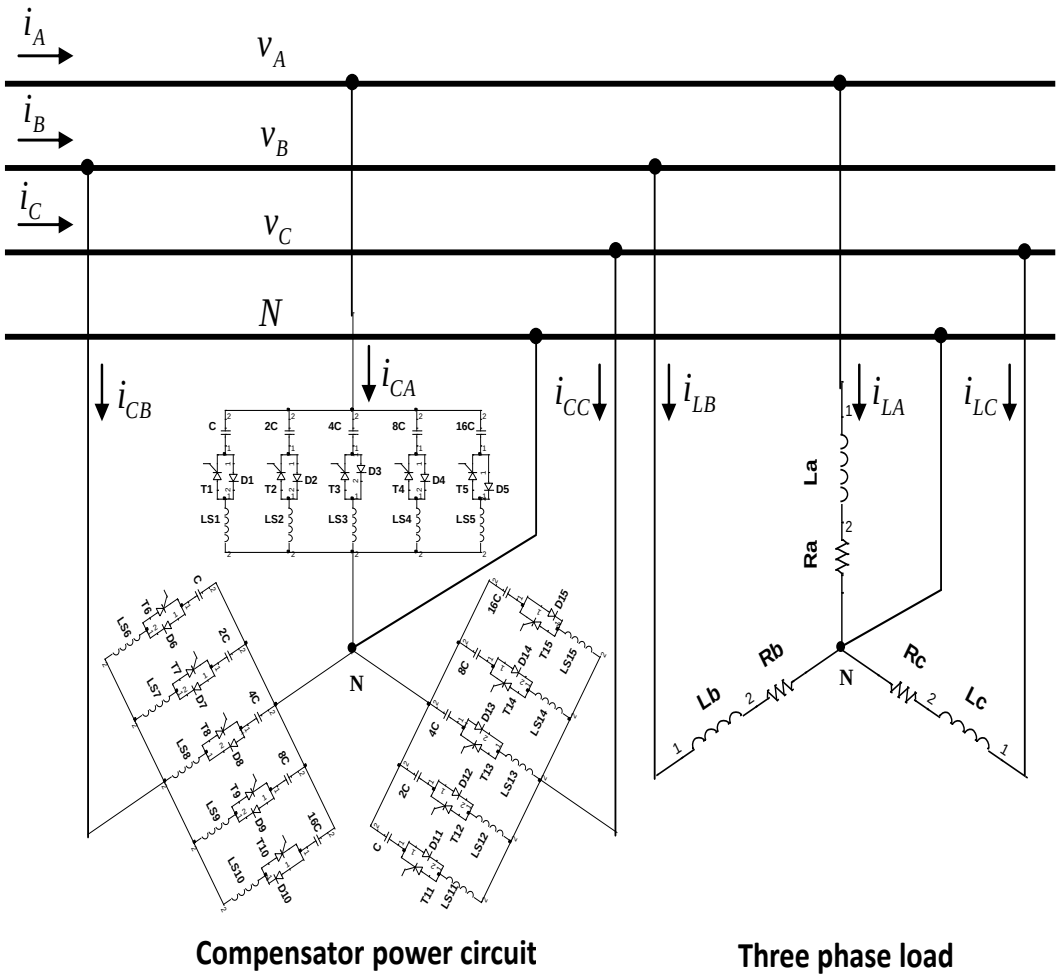

Figure 4. The power circuit of the three-phase power factor correction system.

Figures 6 and 7 show the circuit diagrams of the single-phase and the three-phase automatic power factor correction systems respectively. The simulation results will be extracted from running these systems on PSpice.

RESULTS

The basic capacitance C was chosen to be 50 μF for both single-phase and three-phase systems. The power system network has a frequency of 50 Hz and a phase voltage of 240 volts (r.m.s value). Consequently, the single-phase reactive current rating is 165 A (peak value). Figure 8 shows PSpice tests for the single-phase system.

The first test corresponds to the case at which the load impedance (Z_L) was $1.25\angle 37^o\,\Omega$. The power factor for this load is 0.8 lagging. The reactive component of the load current was 163A (peak value) which was within the compensator rating. Consequently the compensator generated a capacitive reactive current completely cancelled the load current reactive component yielding a real total current (i_T) as shown in Figure 8a. The second test corresponds to an inductive load of $1.25\angle 53^o\,\Omega$. The reactive component for that load was 217.6A (peak value) which exceeded the system rating by 52.6A (peak value). Therefore the power factor for that load was only improved as shown in Figure 8b. Figure 9 shows tests corresponding to the three-phase system.

DISCUSSION

Figure 9a concerns a balanced three-phase inductive

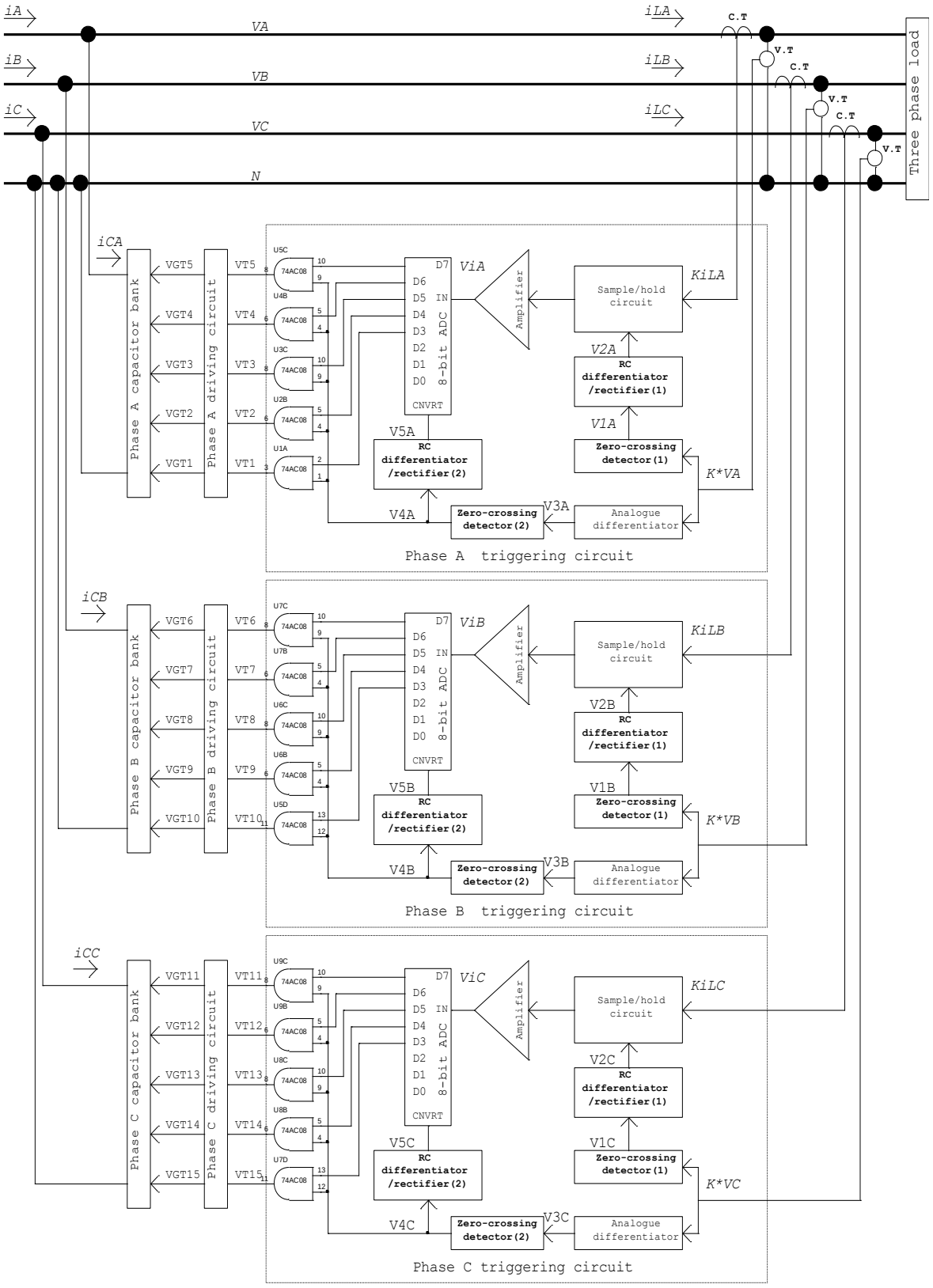

Figure 5. The proposed three-phase power factor correction system scheme.

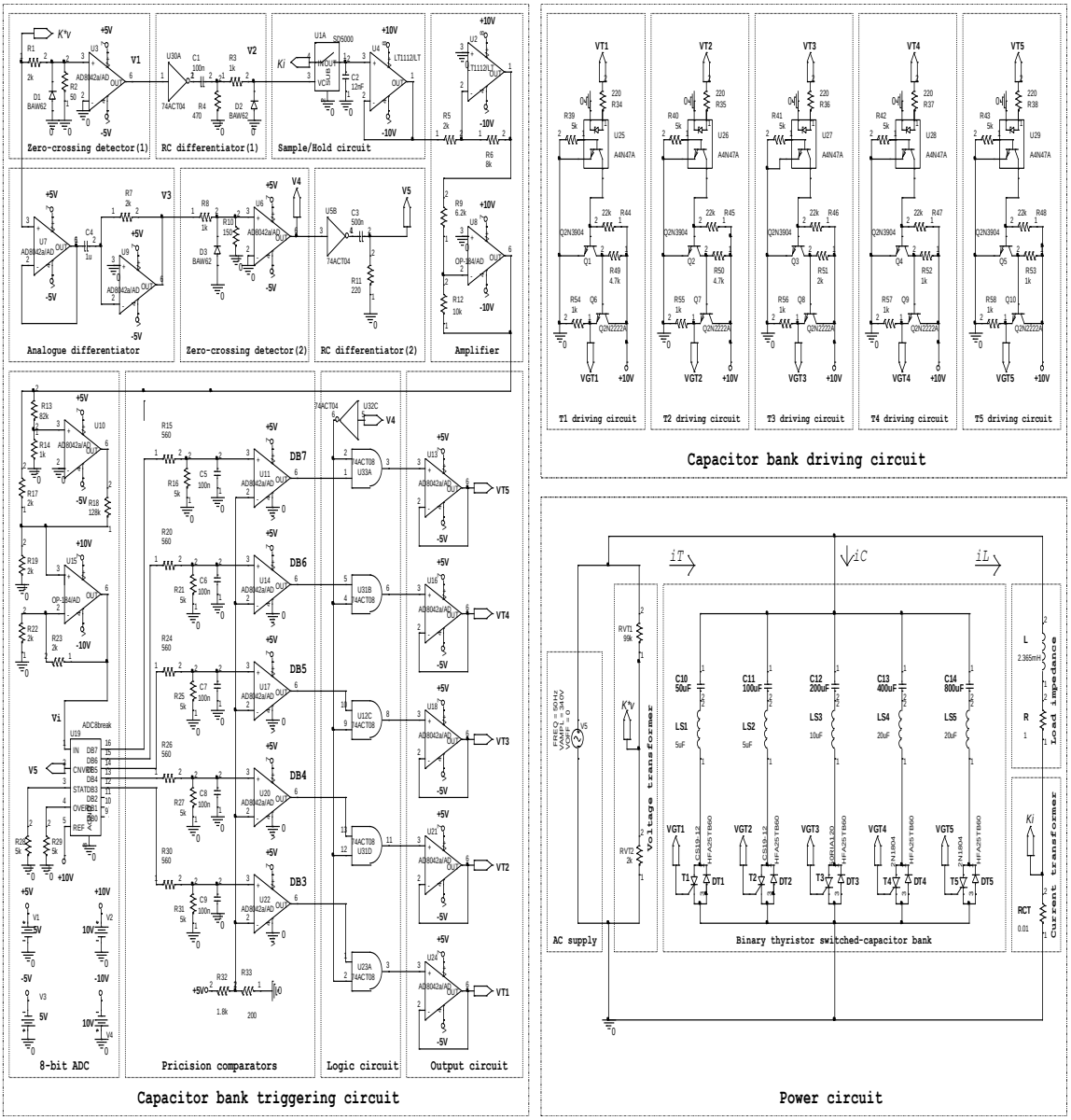

Figure 6. The circuit diagram of the single-phase power factor correction system.

load operating at a 0.8 lagging power factor and exhibiting balanced reactive current components of 163A (peak value). The compensator corrected the power factor to unity for the three-phase load, since the reactive current demands were within its rating. Figure 9b concerns a balanced three-phase inductive load exhibiting balanced reactive current components exceeding the compensator rating, therefore the system was not capable to completely cancel the three-phase reactive current components, but certainly had improved the power factor. Figure 9c shows the response of the three-phase system to a three-phase load balanced in magnitude, but unbalanced in phase. Finally, the compensator was completely relaxed while it was dealing with a balanced three-phase real load as shown in Figure 9d.

Conclusion

The proposed single-phase and three-phase automatic power factor correction systems have certain reactive

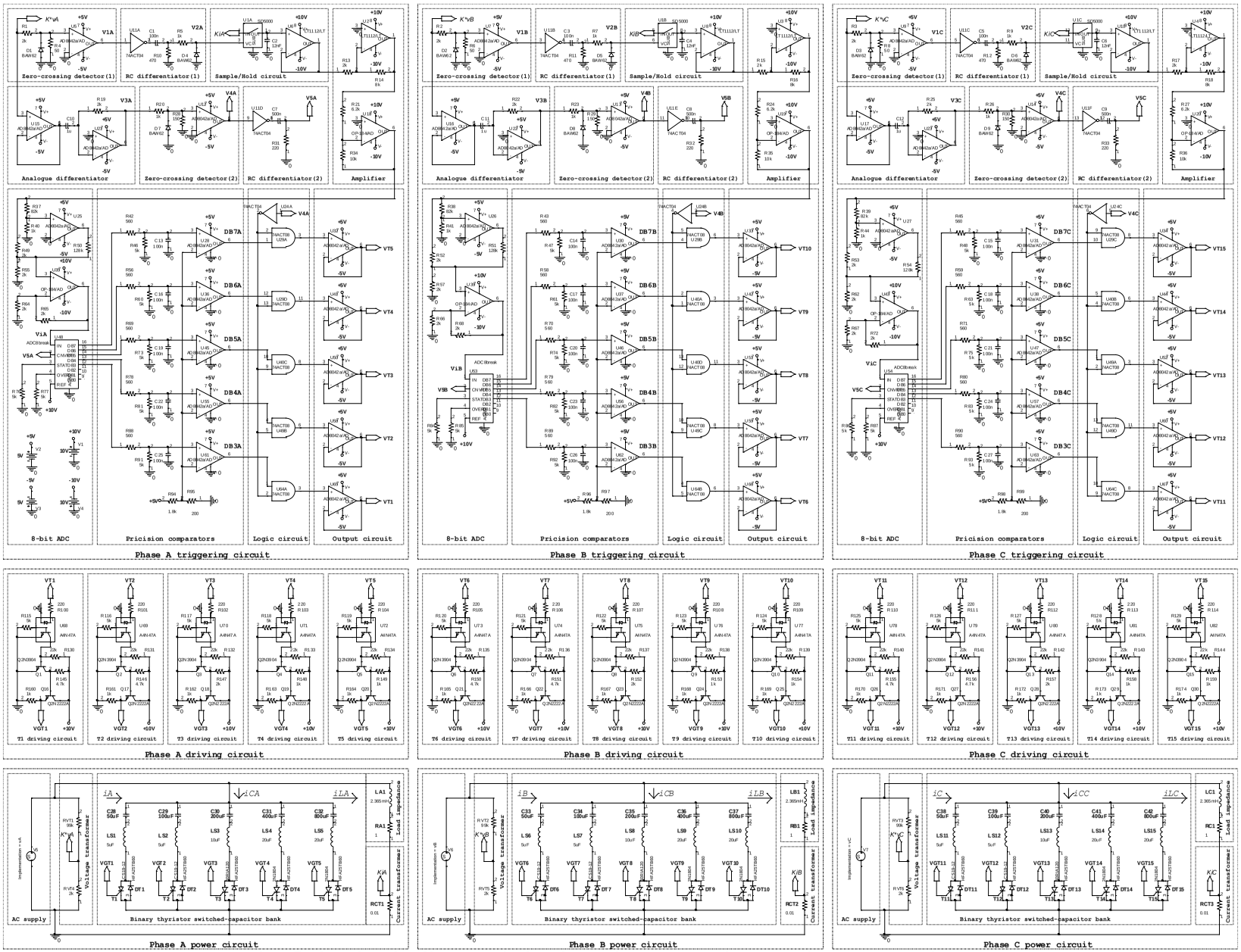

Fig. 7 The circuit diagram of the three-phase automatic power factor correction system.

Figure 7. The circuit diagram of the three-phase power factor correction system.

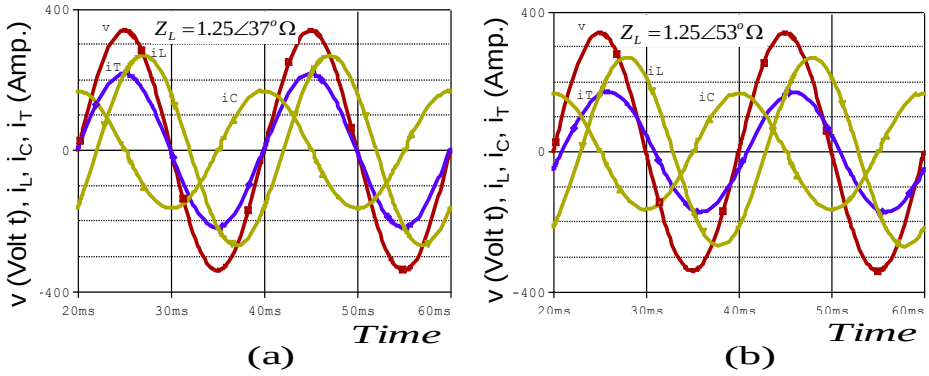

Figure 8. (a) Unity power factor correction, (b) power factor improvement.

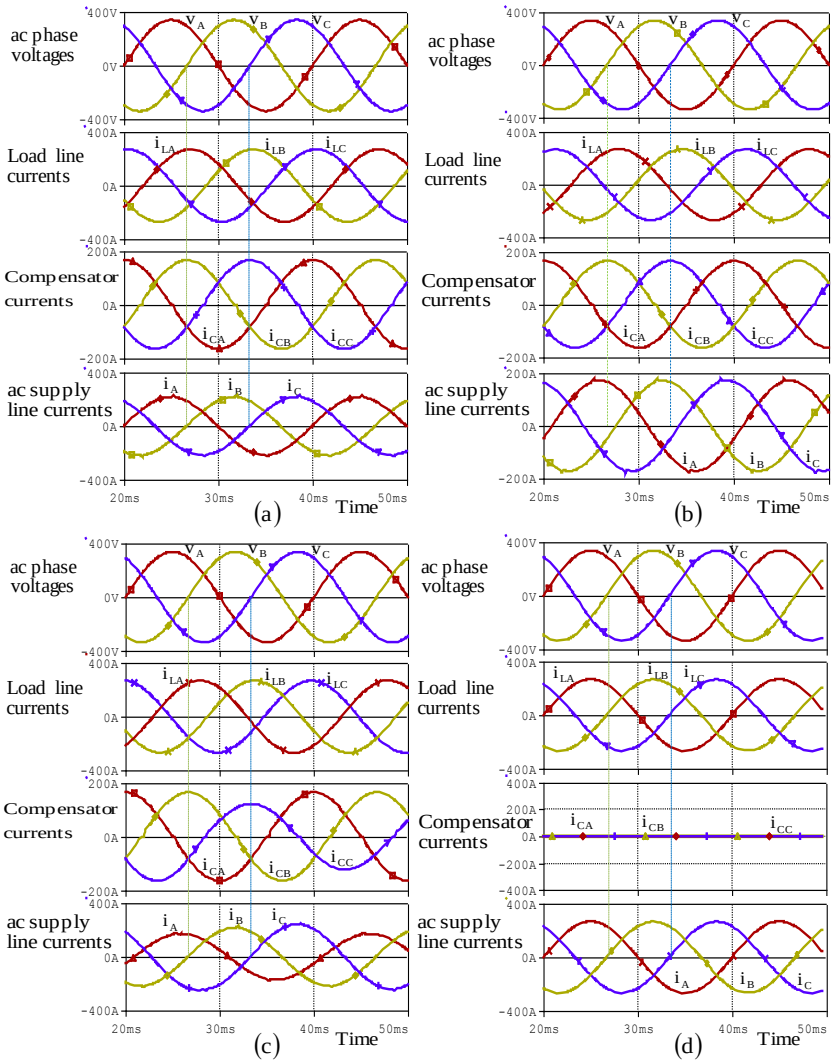

Figure 9. Performance of the three-phase compensator during (a) a balanced full load of 0.8 lagging power factor, (b) a balanced full load of 0.6 lagging power factor, (c) a full load balanced in magnitude and unbalanced in phase, (d) a balanced full resistive load.

current or reactive power ratings. When the detected reactive power absorbed by the load is greater than the compensator rating, the power factor will not be corrected to unity, but certainly will be improved and the apparent power supplied by the ac supply will be reduced. These systems respond almost linearly throughout their pre-assigned areas of operation. They achieve better power quality by reducing the apparent power drawn from the ac supply and minimizing the power transmission losses. In addition, no harmonics disturbing the power system network are released, and hence no filtering is required. The responses of both systems are settled down within the power system network fundamental cycle. There is a feasibility of utilizing this technique for designing systems with high voltage and current ratings. Since this technique is not dealt with accomplishing balanced three-phase currents, the future work will be extended to design an integrated system capable of achieving both power factor correction and load balancing.

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