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Design of a Three-phase Inverter for Variable AC Drive Purposes using a Pulse Width Based on a New Strategy Modulation

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Abstract

In this paper, a pulse width modulation (PWM) technique based on a new strategy is presented first. A three-phase voltage-source inverter based on this technique is then designed for variable AC drive purposes. The new strategy concerns the phase conditioning of the modulating signals such that almost pure sinusoidal balanced three-phase currents are supplied to the induction motor during variable speed operation. The harmonic distortion associating the inverter output currents is negligible. The inverter frequency can be varied from its nominal value (50 Hz) to one-fourth its nominal value (12.5 Hz) keeping constant voltage to frequency ratio. A complete design for this inverter is presented and the whole system is tested on Pspice.

الخلاصة

في هذا البحث تم تقديم أسلوب جديد لتقنية تضمين عرض النبضة. بعد ذلك تم تصميم مقوم عاكس ثلاثي الأطوار يعتمد على هذه التقنية الجديدة ويستخدم لأغراض الدفع المتغير للتيار المتناوب المتغير التردد. الأسلوب الجديد يتعلق بتكييف الإشارة المضمنة بحيث يتم تجهيز تيارات ثلاثية الأطوار متوازنة إلى المحرك الحثي خلال عمليات الاشتغال ذات السرعة المتغيرة. التشوه التوافقي المصاحب لهذه التيارات ضئيل جدا وممكن إهماله. تردد هذا المقوم العاكس قابل للتغيير ضمن المدى(من 50Hz إلى 12.5Hz) مع بقاء نسبة الفولتية إلى التردد ثابتة. تم إجراء عملية تصميم كاملة لهذا المقوم العاكس وتم فحص النظام كاملا باستخدام البرنامج ألتشبيهي (Pspice).

1. Introduction

PWM techniques are used to develop the performance of three-phase inverters such that they approximately yield sinusoidal phase currents. Conventional PWM techniques were applied first on inverters supplying three-phase inductive loads such as induction motors [Rashid 2001, Skkvarenina 2001]. The output currents of those inverters suffered from harmonic distortion and unbalance problem. Many developing strategies were applied on conventional PWM to present new configurations. Some of these new techniques aim to design three-phase inverters capable of supplying loads with phase currents having almost sinusoidal waveforms and small harmonic distortion [Thunes *et al* 1997]. Other techniques are tending to design three-phase inverters yielding three-phase voltages having average values shaping sinusoidal waveforms. The latter techniques are classified into two categories. The first one is dealing with inverters supplied from a single DC voltage source [Jung *et al* 2004]. The microcontrollers used for the gate drives of these inverters are responsible for producing phase voltages having average values forming almost sinusoidal envelopes. The second is dealing with what are known as multilevel three-phase inverters [Tolbert *et al* 2000, Tolbert et al 2002, Mariethoz and Rufer 2004, Chiasson et al 2005, Bao *et al* 2006]. These inverters are cascaded and employing more than one DC voltage source for constituting phase voltages.

Most of the PWM techniques use microcontrollers to design the inverter gate-drive circuitries. For the variable AC drive purposes, the microcontrollers need memories of larger sizes in order to satisfy constant voltage-to-frequency ratio requirements. Here in this work a complete three-phase inverter is designed for driving three-phase induction motor in variable speed mode. No microcontroller is

used and real time operation is employed. The designed inverter is a voltage-source type based on the application of a new strategy on the conventional PWM. This new strategy guarantees sinusoidal phase-currents with constant voltage-to-frequency ratio and negligible harmonic distortion.

2. Single-phase voltage-source inverter based on the new technique

In order to state the design approach of the sinusoidal three-phase inverter, it is better to start the design procedure with a single-phase inverter verifying sinusoidal current output with negligible harmonic distortion. The technique used to achieve such a task is a PWM based on the forward new strategy. Fig.1 shows a single-phase inductive load $Z_L=R_L+jX_L$ supplied by a single-phase voltage-source inverter driven by a controller based on conventional PWM technique. The power factor angle of the load is $\varphi=\tan^{-1}(X_L/R_L)$. $E\sin\omega t$ is a sinusoidal signal of amplitude E and angular frequency $\omega=2\pi f$. Here f represents the inverter main frequency or the frequency of the modulating signal V_{MOD}. V_C is a triangular waveform and is called the carrier signal and its frequency is called the carrier frequency f_C. Note that f_C is much greater than f.

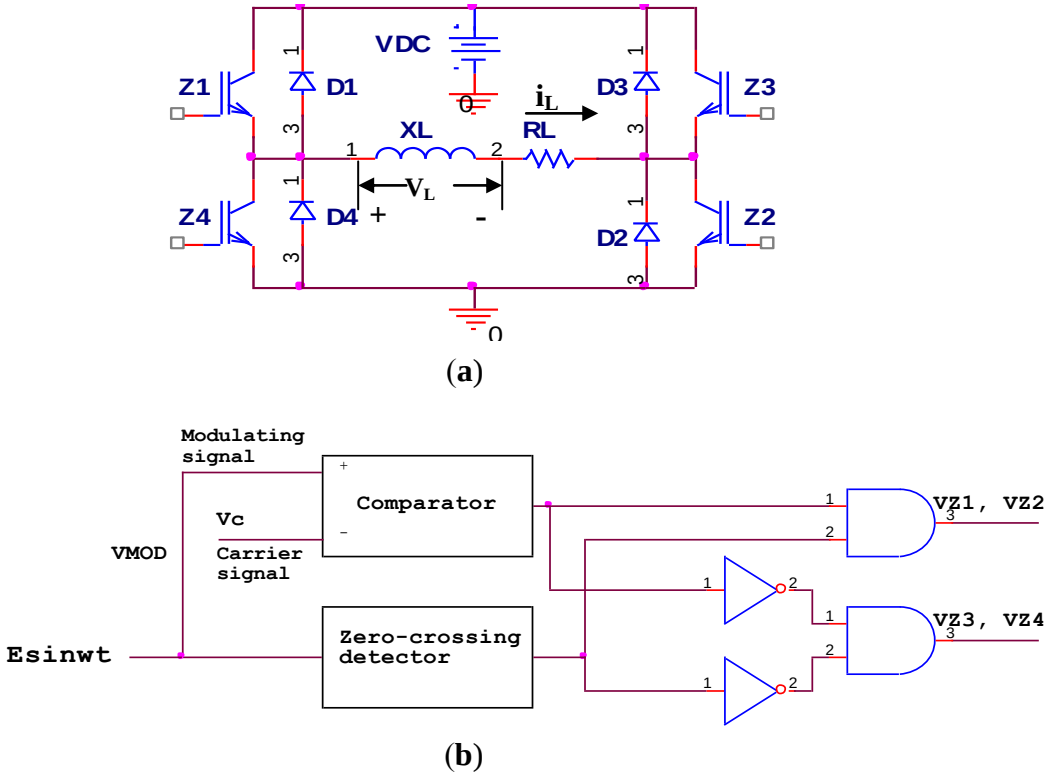


Fig.1 (a) The single-phase voltage source inverter, (b) its conventional PWM circuit.

A load test applied on the inverter of Fig.1 at modulating frequency of 50Hz and a carrier frequency of 1 KHz had given the voltage and current waveforms shown in Fig.2. It is found that the load current i_L is distorted and non-sinusoidal. Now if the PWM circuit is modified such that a lead θ is added to the modulating signal, then

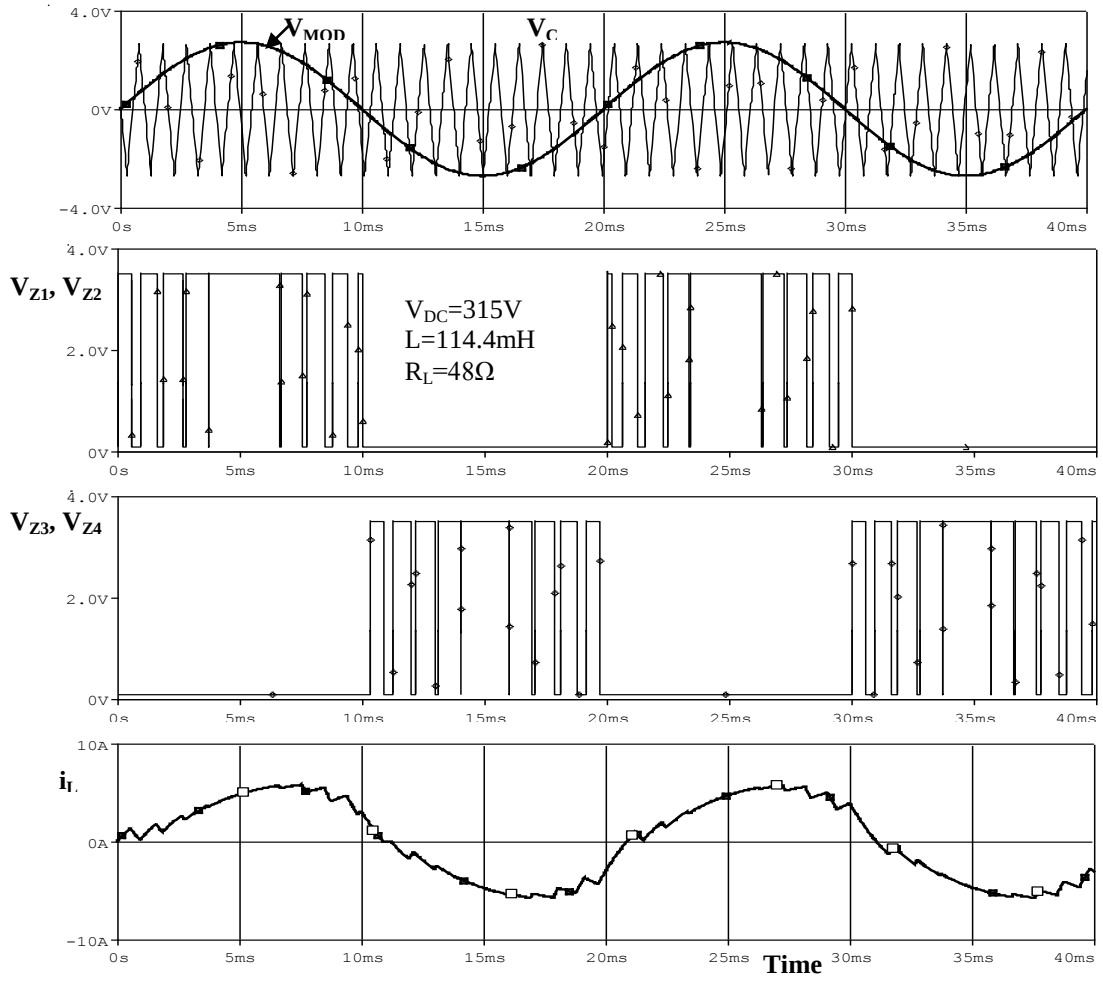


Fig.2 Voltage and current waveforms of a single-phase voltage-source inverter driven by conventional PWM at f_C= 1 KHz and f= 50Hz.

V_{MOD} will equal to Esin (ωt+θ). The modified circuit is shown in Fig.3. Note that the conventional PWM circuit represents the case at which θ=zero. For a value of

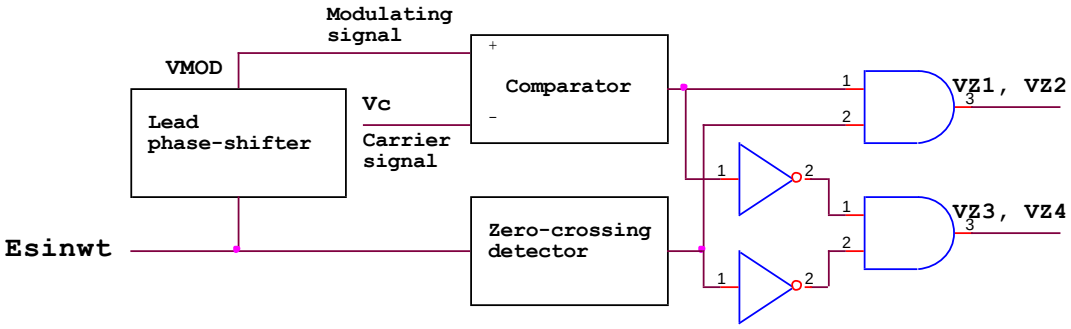


Fig.3 The modified PWM circuit.

θ equal to 90°, a load test is applied. The results for this test are shown in Fig.4. Again, the load current waveform is highly distorted.

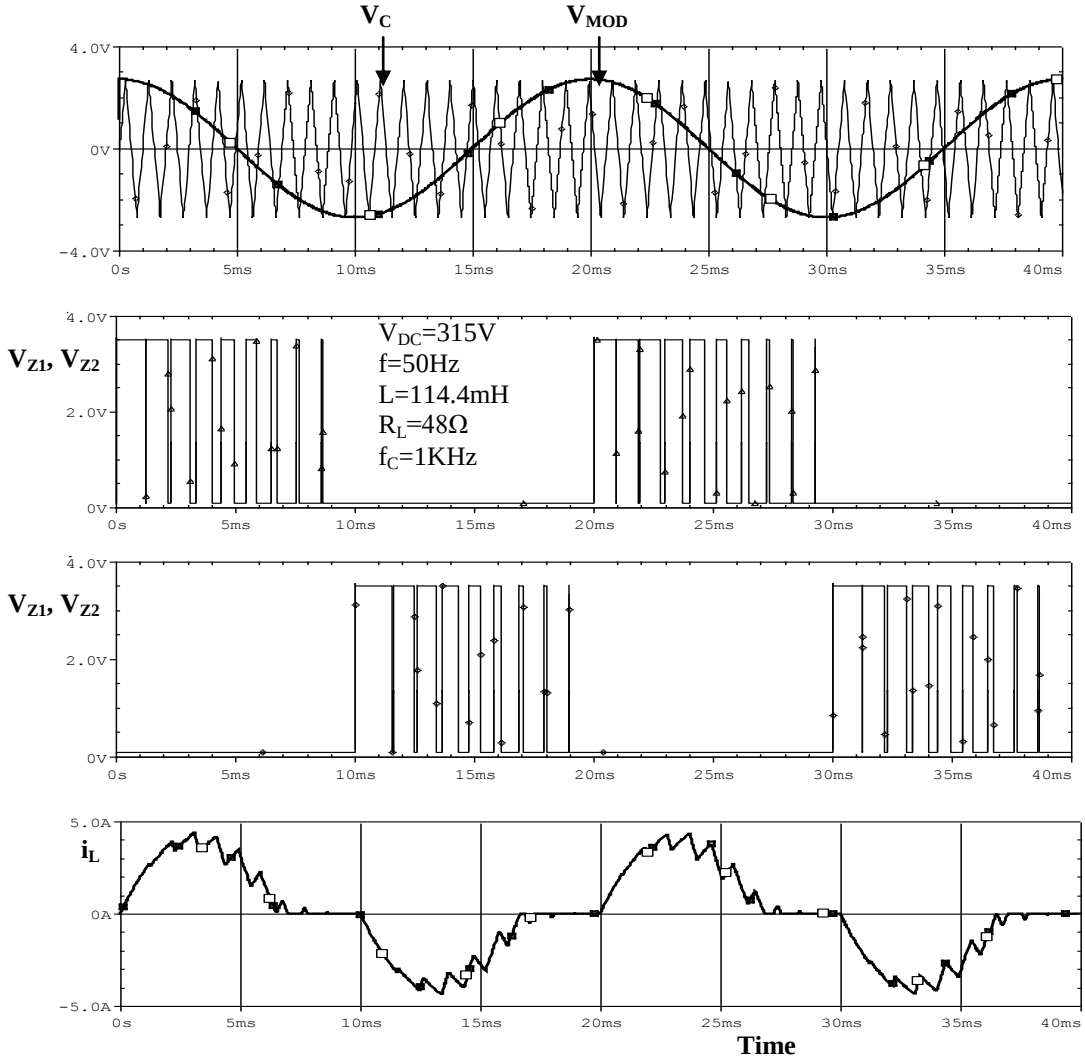


Fig.4 Voltage and current waveforms corresponding to a lead angle θ of 90^o.

Our task is how to find a certain lead angle at which the load current is almost pure sinusoidal with negligible harmonic distortion. Experiments lead to a conclusion that when θ=φ, then this case represents the optimal lead angle. Fig.5 shows a modulating signal having a lead angle equal to φ. As it is seen, the load current has sinusoidal shape and is somewhat symmetrical around the vertical axis. The ripples accompanying the output current waveforms can be easily treated by increasing the carrier frequency f_C.

When the modulating frequency is varied, then the load impedance seen by the inverter will have a new value and this is because the reactive term of Z_L= R_L+j2πfL is frequency dependent. Hence, the power factor angle will have a larger value when the modulating frequency is stepped up and a smaller value when the frequency is stepped down. Consequently, a variable frequency inverter requires a pulse width modulation technique provided with an automatic lead angle control to verify the requirements of sinusoidal current output. For AC drive purposes, a constant voltage to frequency ratio (V/f) is required for constant maximum torque. Hence, the current

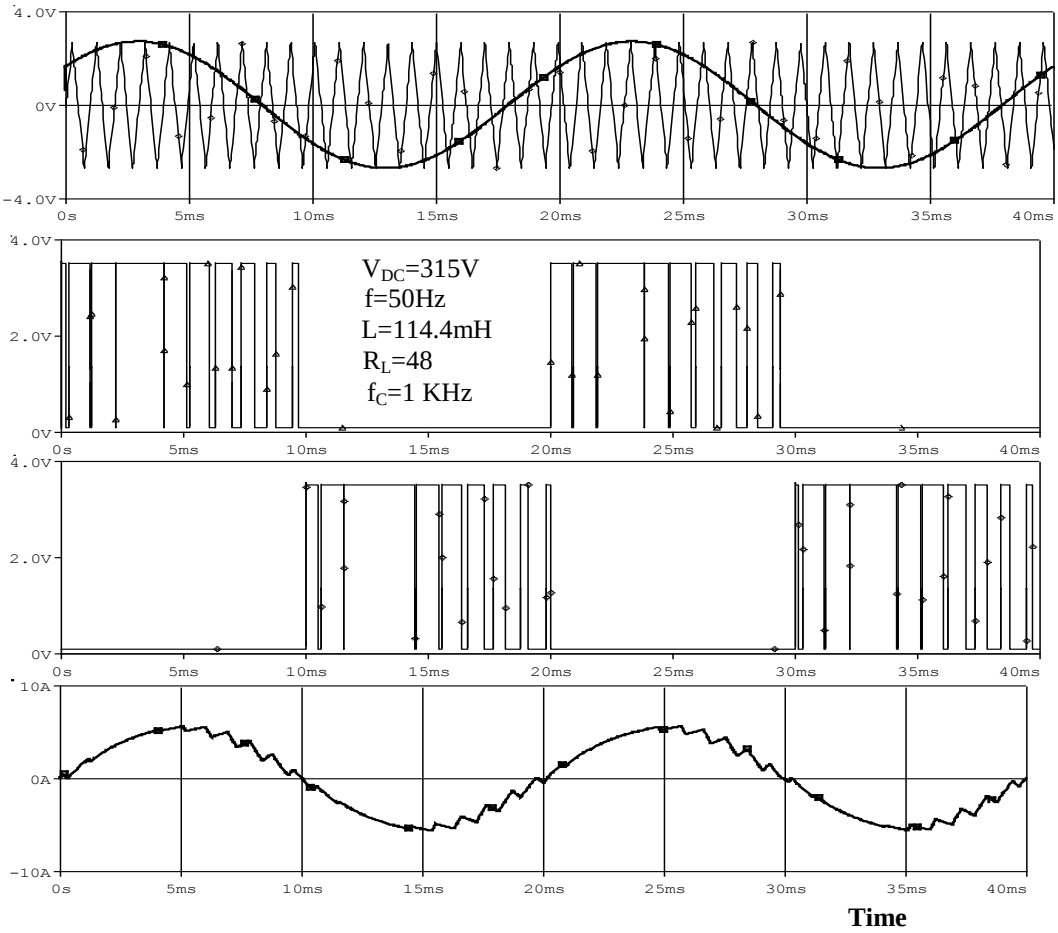


Fig.5 Voltage and current waveforms corresponding to the case where θ=φ.

must be controlled in such a manner that the amplitude of the phase voltage ($V_m=I_m|Z_L|=\sqrt{2}V$) will verify a constant voltage to frequency ratio.

2.1 The modified PWM circuit design

Fig.6 shows the modified single-phase PWM circuit. This circuit is provided with a frequency dependent lead phase-shifting network and a carrier signal generator governing its output amplitude according to the modulating frequency f. The lead phase-shifting network is designed in such a manner that the sinusoidal waveform will suffer a lead phase-shift equal to the power factor angle φ of the load impedance at the operating frequency f.

The nominal modulating frequency f_o for the modified single-phase PWM circuit is chosen to be 50Hz and the variation range of this frequency is restricted within 50Hz to 12.5Hz. This leads to the possibility of induction motor speed control range from rated value to one fourth its rated value. An inductive load of 0.8 lagging power factor is a reasonable steady state representation of a single-phase induction motor at the nominal frequency f_o. The sinusoidal waveform generation circuit is composed of two sub circuits; the first is generating a triangular waveform and the second is converting the triangular waveform to a sinusoidal one at the same frequency. The frequency of this waveform is given by [Millman and Halkias 1983]

$$f = \frac{R_3}{4(R_1+R_2)R_4C_1} \quad \text{..... (1)}$$

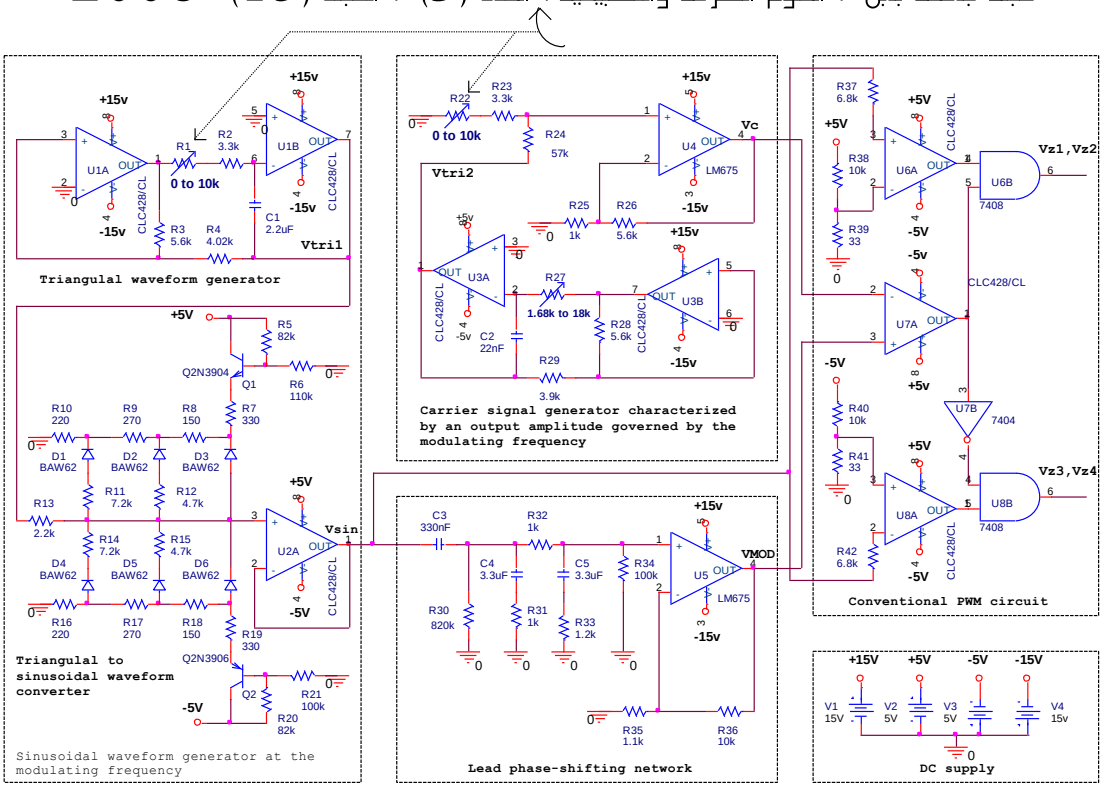


Fig.6 The modified PWM circuit for variable AC drives.

Zero setting of R_1 yields a frequency of 50Hz, while 10k setting corresponds to a frequency of 12.5Hz. Note that when the circuit parameters R_1, R_2, R_3, R_4, and C_1 values in Fig.6 are directly substituted in equation(1) then the frequency f will be a bit smaller than practical one. This is because of the internal parameters of the operational amplifier U1A and U1B, which are taken into account during design process. The triangular to sinusoidal waveform conversion is done properly by accurate determination of circuit parameters, definitely the quiescent points of the signal diode D_1, D_2, D_3, D_4, D_5, and D_6.

The lead phase-shifting circuit introduces a lead phase-shift depending on the frequency of the sinusoidal input voltage V_{sin}. The overall voltage gain of this circuit is closely approximated to:

$$\text{..... (2)} \quad Gain = \frac{V_{MOD}}{V_{\sin}} = \frac{10.1(1+j0.025f)^2}{22-0.00175f^2+j0.825f} = K_1\angle\theta$$

Where K_1 is the absolute value of the gain and is given by

$$K_1 = \frac{10.1(1+0.000625f^2)}{\sqrt{(22-0.00175f^2)^2+0.6806f^2}} \quad \text{..... (3)}$$

θ is the phase lead angle and is given by

$$\text{..... (4)} \qquad \theta = 2\tan^{-1}(0.025f) - \tan^{-1}\left(\frac{0.825f}{22-0.00175f^2}\right)$$

The practical measurements of this circuit had given the results shown in Table (1).

Table (1) K_1 and θ variations against the modulating frequency f

Frequency (Hz)	Absolute gain (K_1)		Lead phase angle (θ) in degrees	
	Measured	Calculated	Measured	Calculated
50	0.5951	0.5770	37.80	35.84
40	0.5437	0.5300	30.24	30.20
33.333	0.5187	0.5027	27.00	25.70
25	0.4936	0.4800	20.61	18.62
20	0.4837	0.4700	16.20	15.37
12.5	0.4767	0.4610	10.38	9.40

The calculated values of K_1 and θ are directly obtained from equations (3) and (4). They are a bit smaller than those obtained by direct measurements. This is because of ignoring the internal parameters of the operational amplifier U5 and the resistance R_{34} during the voltage gain determination. Note that the measured values of θ are quite coinciding with the power factor angle φ of the load impedance. Note that the power factor of the inductive load is 0.8 at the nominal frequency (50Hz).

The carrier signal generator includes two sub circuits; the first is an adjustable frequency triangular waveform generator, and the second is a governed non-inverting amplifier. The voltage gain of this amplifier is given by

..... (5)

$$K_2 = \frac{(R_{22}+R_{23})}{(R_{22}+R_{23}+R_{24})}\left(1+\frac{R_{26}}{R_{25}}\right) = 6.6\frac{(R_{22}+3300)}{(R_{22}+60300)}$$

The variable resistance R_{22} is mounted on the same shaft with the resistance R_1, which is governing the inverter modulating frequency f. Since R_1 and R_{22} are matched, K_2 will be modulating frequency dependent and this is clearly indicated in Table (2).

Table (2) K_2 variations against the modulating frequency f

$R_{22}=R_1$ (KΩ)	Modulating Frequency (Hz)	K_2 Measured
0	50	0.361
0.866	40	0.450
1.700	33.33	0.532
3.350	25	0.690
5.035	20	0.842
10	12.5	1.249

The conventional PWM circuit compares the modulating signal V_{MOD} with the carrier signal $V_{C.}$ The output of the comparator U7A is dependent on the amplitudes of both signals. $V_{MODpeak}= K_1V_{sinpeak}$ and $V_{Cpeak}=K_2V_{tr2peak}$. The circuit of Fig.6 is designed such that $V_{sinpeak}=1.72V$ and $V_{Cpeak}=2.72V$. $V_{MODpeak}$ to V_{Cpeak} ratio is governing the voltage-to-frequency ratio and is denoted by K, which is given by

..... (6)

$$K = \frac{V_{MODpeak}}{V_{Cpeak}} = \frac{1.72K_1}{2.72K_2} = 0.6324\frac{K_1}{K_2}$$

Table (3) shows the variation of K with the inverter main frequency f. The building up of load current is dependent on the load impedance time constant $\tau = L/R_L$ and the status of the PWM signal which is coherently affected by the value of K. A single pulse of a PWM train is a rectangular waveform. Its positive portion is called T_{on} and its negative potion is called T_{off}. T_C denotes the repetition time of this waveform, and is equal to $1/f_C = T_{on} + T_{off}$. When T_{on} is so much greater than T_{off}, then the load current will hastily build up in magnitude. If T_{on} is less than T_{off}, then the load current will build down in magnitude.

Table (3) K variations against f

f (Hz)	K_1	K_2	K
50	0.5770	0.361	1.012
40	0.5300	0.450	0.917
33.33	0.5027	0.532	0.600
25	0.4800	0.690	0.440
20	0.4700	0.842	0.353
12.5	0.4610	1.249	0.233

All the circuit parameters of Fig.6 are determined taking into account an inductive load of 0.8 power factor at the nominal frequency f_o=50Hz. Hence, the load impedance at f_o can be written as: $Z_L(f_o)=|Z_L(f_o)|(0.8+j0.6)$, where $|Z_L(f_o)|$ is the absolute value of the load impedance at f_o. If a factor n is defined as $n=f/f_o$, then the absolute value of the load impedance at any frequency is given by

$$|Z_L(f)| = |Z_L(f_o)|\sqrt{0.64 + 0.36n^2} \quad \text{..... (7)}$$

To keep constant voltage to frequency ratio, the ratio of the phase voltage at f_o to the phase voltage at any frequency must equal to 1/n. This can be written as:

$$\frac{I_L(f_o)|Z_L(f_o)|}{I_L(f)|Z_L(f_o)|\sqrt{0.64 + 0.36n^2}} = \frac{1}{n} \quad \text{, or}$$

$$I_L(f) = \frac{n}{\sqrt{0.64 + 0.36n^2}} I_L(f_o) \quad \text{..... (8)}$$

Where $I_L(f)$ and $I_L(f_o)$ are the rms values of load currents at f and f_o respectively. When the inverter is required to operate at 12.5 Hz, which represents the minimum operating frequency for this inverter, then $I_L(12.5)=0.307I_L(50)$. This explains the minimum value of K at 12.5Hz as stated in Table (3).

The carrier frequency f_C of the circuit of Fig.6 can be varied from less than 1 KHz up to 10 KHz, by adjusting the potentiometer R_{27}. As f_C increases, the load current will be smooth sinusoid. The designer must restrict this frequency when the design process is over. So far, the single-phase approach of the new strategy is done.

3. Three-phase design procedure

The single-phase modified PWM circuit can be generalized to build the three-phase PWM circuit. Since, a complete three-phase circuit diagram is required; the

design process must introduce the full hardware to install the whole system. A three-phase Y-connected squirrel-cage induction motor is selected as a balanced three-phase load for this inverter. The ratings of the induction motor must be specified in order to determine the inverter ratings. A 7.5KVA, 50Hz, 1450rpm, 380V, 11.4A, 0.8-p.f induction motor is selected as a load. A 630V DC supply is sufficient to make the inverter produce the average line-to-line peak voltage ($380*\sqrt{2}=537.4V$). Six IGBT modules of the type 1XGH 10 N100A are selected as solid-state switching devices. Each module includes one insulated-gate bipolar transistor (IGBT) shunted by a reverse fast recovery epitaxial diode (FRED). Fig.7 shows the block diagram of the three-phase inverter, which is driven by the modified PWM circuit and designed for

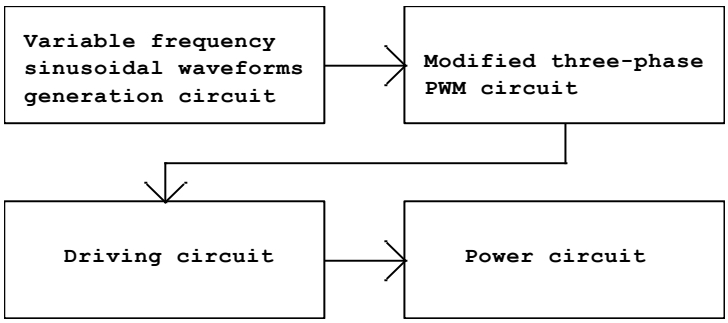


Fig.7 The block diagram of a three-phase inverter designed for variable AC drive purposes and driven by the modified PWM circuit.

variable AC drive purposes. The sinusoidal waveforms generation circuit produces three-phasor voltages; $1.72\sin\omega t$, $1.72\sin(\omega t-120^o)$, and $1.72\sin(\omega t-240^o)$. Where $\omega=2\pi f$ and f represents the inverter main frequency or the modulating frequency. The frequency f can be varied from 50Hz to 12.5Hz. These phasor-voltages are employed in the modified three-phase PWM circuit to produce the triggering signals required for the solid-state switching devices. The driving circuit includes six individual sub circuits. The power circuit consists of six IGBT-modules, a 630V DC voltage, and a three-phase inductive load representing the proposed three-phase induction motor.

4. The three-phase circuit design

A complete three-phase circuitry is designed for a three-phase inverter driven by the modified PWM circuit. Fig.8 shows the complete circuitry of this inverter. The circuit diagram is divided into four blocks coinciding with those of Fig.7. Each block includes one of the main circuits of the inverter. Obviously, these circuits are divided into sub circuits. Each sub circuit performs a certain function. The sinusoidal waveforms circuit consists of five sub circuits. The first one is a triangular waveform generator. Its output has an adjustable frequency f and constant amplitude of 2.8V and is designated by V_{S1}. Its frequency represents the inverter main frequency or the modulating frequency, which can be smoothly varied from 50Hz to 12.5Hz by adjusting the potentiometer R_1. The second sub circuit is an active network designed in such a manner that the input signal V_{S1} will suffer a time delay of T/4 and its output is denoted by V_{S2}. The third and the fourth sub circuits are identical precision triangular-to-sinusoidal waveform converters and their outputs are $1.72\sin\omega t$ and $1.72\sin(\omega t-90^o)$ respectively. The fifth sub circuit is a summing network producing $1.72\sin(\omega t-120^o)$ and $1.72\sin(\omega t-240^o)$. Hence this circuit generates the small signal three-phase voltages $V_{P1}=1.72\sin\omega t$, $V_{P2}=1.72\sin(\omega t-120^o)$, and $V_{P3}=1.72\sin(\omega t-$

Fig.8 The circuit diagram of the almost pure sinusoidal three-phase inverter designed for AC variable-drive purposes.

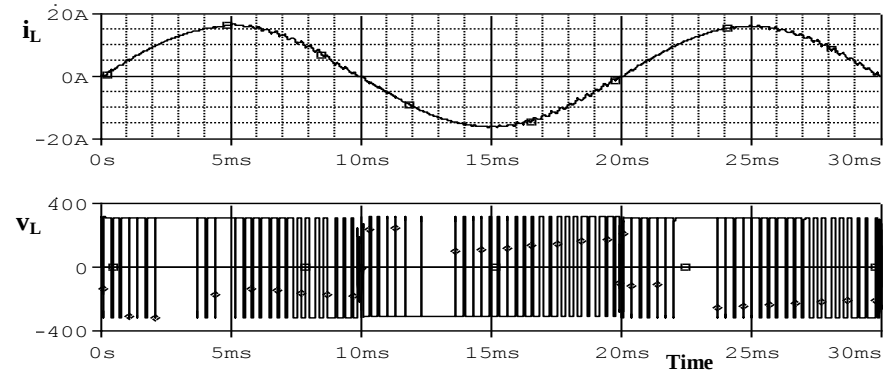
240^o). The second main circuit represents the modified three-phase PWM circuit. It consists of four sub circuits. The first one is a triangular waveform generator followed by a non-inverting amplifier having a voltage gain K_2 specified in table 2. The output of this sub circuit represents the carrier signal V_C, which has the frequency f_C. This frequency can be adjusted by the individual potentiometer R_{71}. The value of K_2 is governed by the potentiometer R_{74}. Note that R_{74} and R_1 are matched and mounted on the same shaft. The second sub circuit consists of three lead phase-shifting networks and three comparators. Each lead phase-shifting network is identical to that introduced in Fig.6. The outputs of these networks are the modulating signals V_{MOD1}, V_{MOD2}, and V_{MOD3}. These signals are compared with the carrier signal V_C to produce the pulse width modulated signals V_{PW1}, V_{PW2}, and V_{PW3}. The third sub circuit consists of three almost +0 detectors and three almost -0 detectors to the phasor voltages V_{P1}, V_{P2}, and V_{P3}. The positive detectors compare these phasor voltages with about 16.5mV DC level, while the negative detectors compare a negative DC level of about -16.5mV with the same phasor voltages. The positive detectors produce the rectangular waveforms V_{PPZ1}, V_{PPZ2}, and V_{PPZ3}, while the negative detectors produce the rectangular waveforms V_{PNZ1}, V_{PNZ2}, and V_{PNZ3}. The positive portion of each of these rectangular waveforms is less than the negative portion. This is to avoid instantaneous commutations of the switching devices of each inverter leg. The fourth sub circuit is a digital circuit investing the three-pulse width modulated signals of the second sub circuit and the six rectangular waveforms of the third one to produce the six PWM triggering signals V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, and V_{Z6}. Each triggering signal is leading its next one by 60^o. The third main circuit is the driving circuit. It consists of six similar sub circuits. Each of them concerns one switching device. They are designed such that the driven switching devices will be snubberless. This means that these driving circuits safely treat di/dt and dv/dt. In addition, they are limiting the total switching energy loss of each IGBT to be less than typical values. Note that the typical total switching energy loss of the IGBT used in this inverter is about 3.6mJ at 25C^o. The opto couplers offer electrical insulations between low DC voltages and high DC voltages. The final main circuit is the power circuit. It includes two sub circuits. The first one consists of six IGBT-modules and a 630V DC voltage. For Pspice simulator purposes the effect of stray inductance is treated by adding a 100nH inductor in series with V_{DC}. Each IGBT-module includes one IGBT and a fast recovery free-wheel diode. The IGBT is of the type 1XGH10N100A and its ratings at 25C^o are V_{CEmax}=1000V, I_{Cmax} (continuous) =20A, I_{Cmax} (pulsating) =40A, V_{GEmax}=±20V, V_{CEsat}=3.5V, and P_{Cmax}=100W. The second sub circuit is the steady-state representation of the proposed three-phase induction motor

The circuit parameters of Fig.8 are carefully optimized and then specified to their circuit elements. The whole system was experimented on Pspice simulator and successful results were obtained.

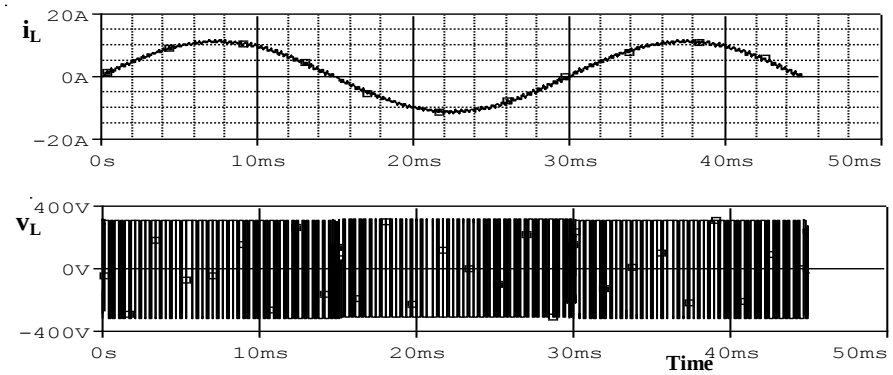
5. Results and conclusions

The single-phase and the three-phase inverters were tested on Pspice at 27C^o. The single-phase inverter load is an inductive load representing one-phase impedance of the selected three-phase induction motor. The power circuit of the single-phase inverter is the circuit shown in Fig.1a. The DC voltage of this inverter is 315V. The modified PWM circuit shown in Fig.6 drives this voltage-source inverter. The single-phase inverter was tested at a carrier frequency of 3 KHz and a variable modulating frequency within the range of 50Hz to 12.5Hz. Fig.9 shows the results of these tests.

Note that the average value of the phase-voltage v_L corresponding to each test is sinusoidal. The dotted sinusoidal waveform of Fig.10 obviously indicates this fact.



(a)



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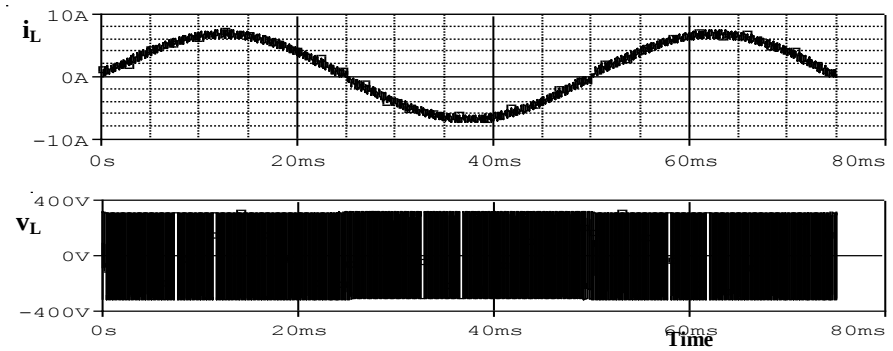

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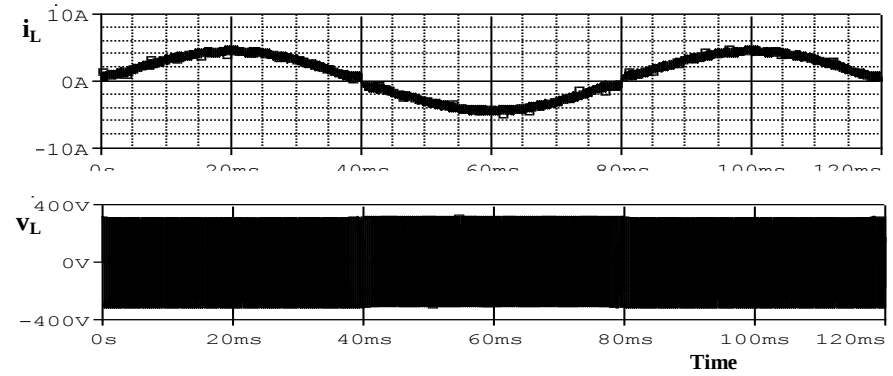

(d)

Fig.9 Single-phase inductive load tests at different modulating frequencies.

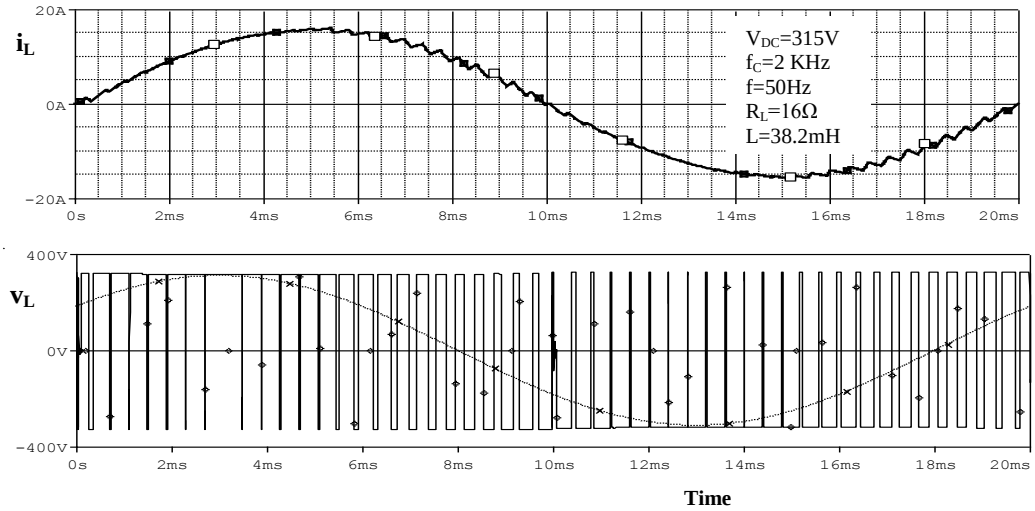

Fig.10 A single-phase inductive load test shows that the phase voltage average values constitute a sinusoidal waveform.

The phase voltages at different frequencies are obtained directly by multiplying the rms values of the load currents at these frequencies by their corresponding load impedances. The voltage-to-frequency ratio variations against frequency are shown in Fig.11. It is clear that this ratio is almost constant. The maximum error associating the voltage-to-frequency ratio curve is less than 4 percent. This offers the proper condition for constant maximum torque. It is possible to vary the carrier frequency until 10 KHz. Above 10 KHz, the total switching energy loss for each IGBT used in this inverter exceeds its typical value and this may constitute a real risk to the inverter. Large carrier frequency leads to smooth sinusoidal load current. This frequency must not be varied while the inverter is supplying power to the load.

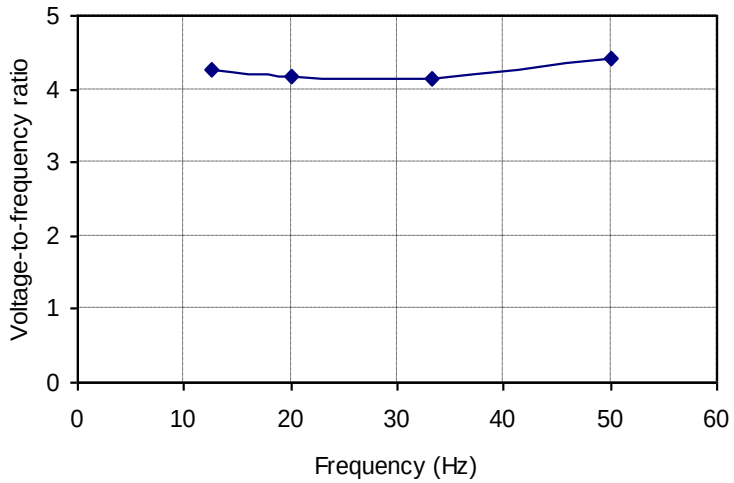

Fig.11The single-phase voltage-to-frequency ratio against frequency.

Fig.12, Fig.13, and Fig.14 show three-phase load tests applied at different modulating frequencies. These tests were applied on the three-phase inverter shown in Fig.8 at a constant carrier frequency of 3 KHz. Two of these tests were applied at the extremes of the inverter frequency band and the third was applied one octave apart from both extremes. It is clearly seen that the load currents in all these tests are balanced and 120^o phase-shifted from each other. Hence, the rms value of the phase

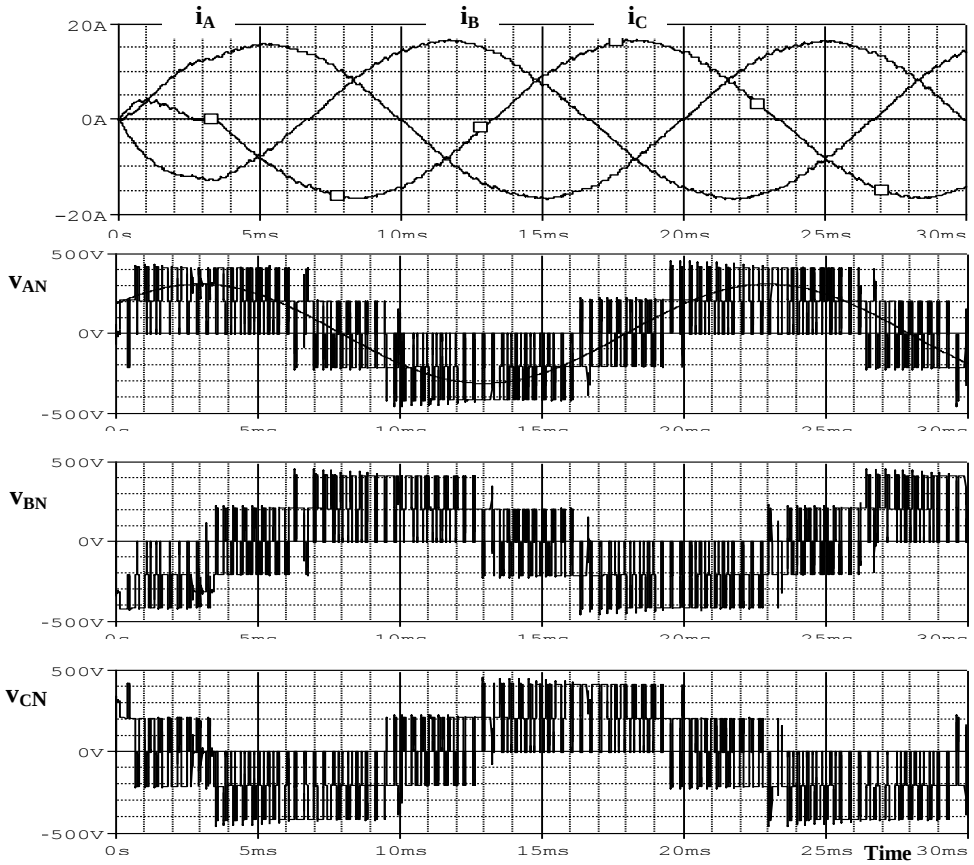

Fig.12 A three-phase load test applied at f= 50Hz and f_C= 3 KHz.

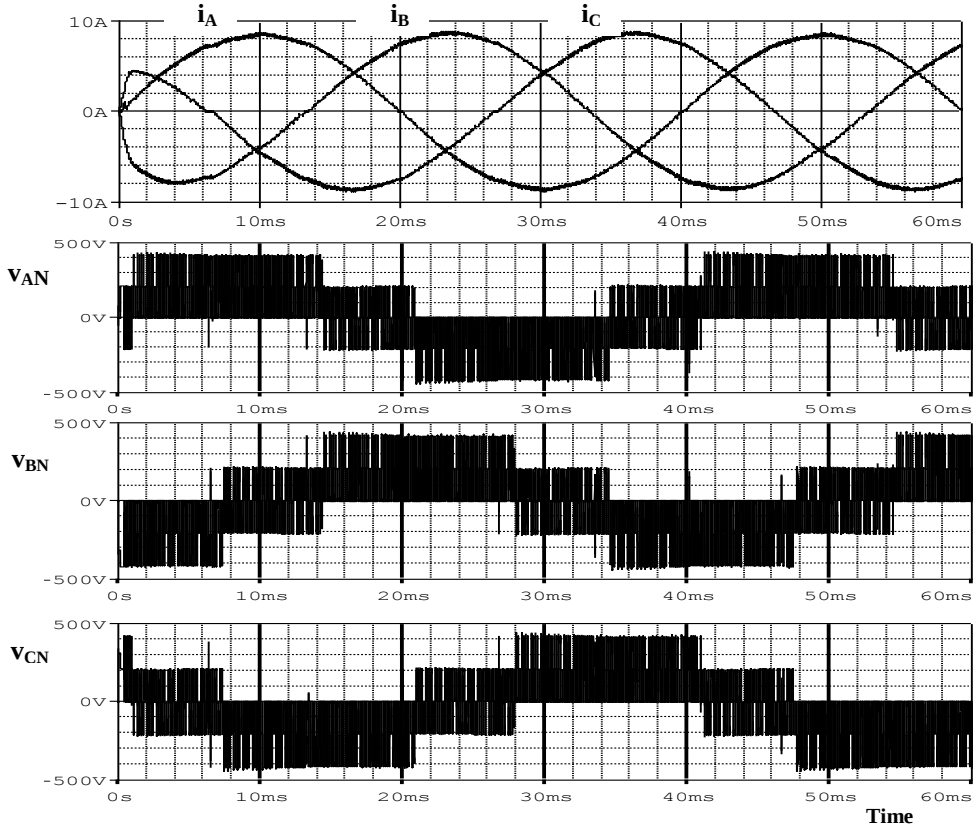

Fig.13 A three-phase load test applied at f= 25Hz and f_C= 3 KHz.

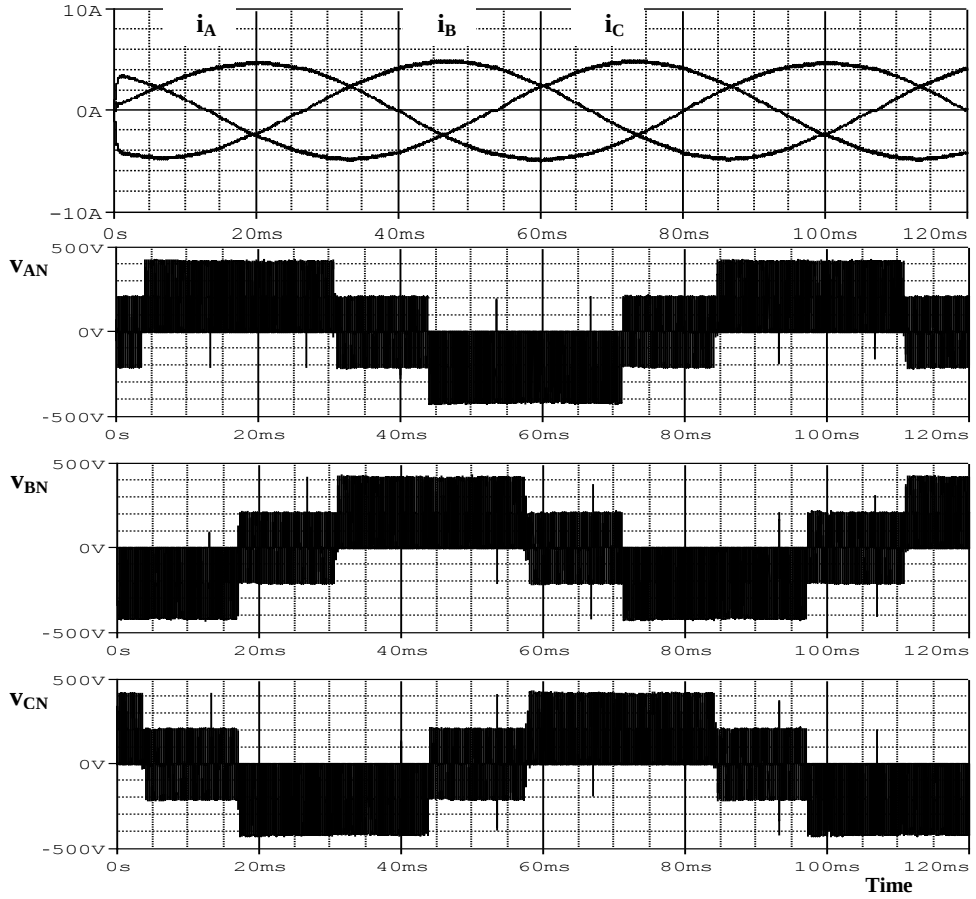

Fig.14 A three-phase load test applied at f= 12.5Hz and f_C= 3 KHz.

voltage for each test is directly obtained by multiplying the rms value of the phase current by its corresponding phase impedance. Fig.15 shows the curve of voltage-to-frequency ratio against frequency for these tests. The maximum error associated with the voltage-to-frequency ratio is less than 4 percent and this situation guarantees the requirements for constant maximum torque.

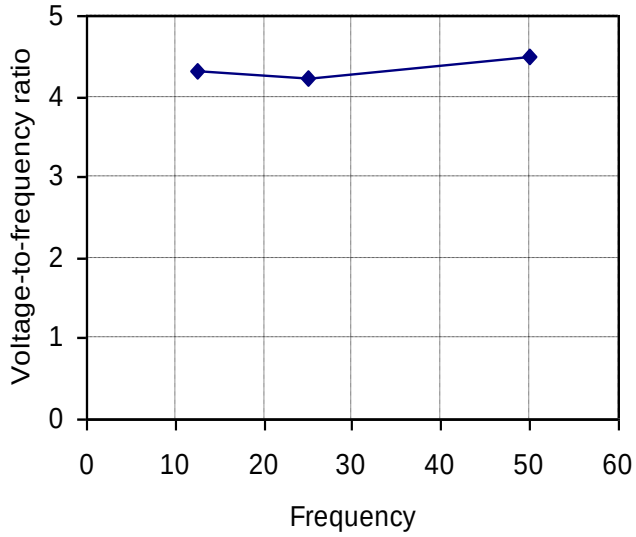

Fig.15 The plot of the voltage-to-frequency ratio versus frequency corresponding to the three-phase load tests.

The phase current waveforms of Fig.12, Fig.13, and Fig.14 seem somewhat distorted at the first half cycles and this is because of the nature of inductance current, which always starts from zero. The sinusoidal waveform appearing on the phase voltage v_{AB} of Fig.12 denotes the envelope constituted by its average values. The envelopes of the average values of the phase voltages v_{AN}, v_{BN}, and v_{CN} are leading their corresponding phase currents i_A, i_B, and i_C by the lead angle θ which is equal to the power factor angle φ.

The above tests assume the steady-state operation of the induction motor. During the starting conditions, the phase impedance of the induction motor become more resistive than its steady-state value and this is because the starting slip is much greater than steady-state slip. More resistive impedance means less time constant and this leads to the building up of phase currents having larger values sufficient for producing the required starting torque. The phase starting currents are taken into account during the design process. The IGBTs used in this inverter have pulsating current ratings more than their continuous ratings. This offers a good protection for each IGBT against starting currents.

The three-phase inverter designed here is characterized by its fast response and this is due to its real time operation. It is possible to produce very smooth sinusoidal phase currents by increasing the carrier frequency above 3 KHz. Finally, the three-phase vision of the new strategy has been fulfilled. This work can be modified to comprise the operation with random loads by adding certain hardware capable of detecting the load power factor and then creating the required lead phase shifting to the modulating signals.

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