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Design of a Three-Phase Statcom-Based Inductive Static VAR Compensator Using DC Capacitor Voltage Control Scheme

Abdulkareem Mokif Obais and Jagadeesh Pasupuleti
Department of Electrical Power Engineering, Universiti Tenaga Nasional, Malaysia

Abstract: In this study, a three-phase continuously controlled harmonic-free inductive static VAR compensator is presented. The compensator is built of a three-phase voltage source inverter based statcom. The phase currents of this compensator are linearly and continuously controlled by the statcom DC capacitor voltage. The control strategy is outlined by a process of forcing the capacitor voltage to follow a certain reference voltage which can be varied linearly from its maximum to its minimum values to produce balanced three-phase inductive currents varying in the range of zero to maximum value (I_{MAX}). The proposed compensator was verified on the computer program PSpice.

Keywords: Controlled reactors, power quality, reactive power control

INTRODUCTION

Static VAR compensators have significant impacts on power quality improvement. They are playing very important roles in voltage control, minimization of transmission losses, power factor improvement, stability of power systems and load balancing (Singh *et al*., 2008; Slepchenkov *et al*., 2011; Xu *et al*., 2010; Wolfle and Hurley, 2003; Peng, 1998). Both generation and absorption of reactor power are important in power quality improvement. Compensators employing switched-capacitors are harmonic-free static VAR generators and are characterized by stepping responses (Jintakosonwit *et al*., 2007). A Thyristor Controlled Reactor (TCR) is a continuously controlled static VAR absorber, but it generates wide spectrum of odd current harmonics, thus it needs harmonic filtration techniques (Yacamini and Resende, 1986; Haque and Malik, 1987). Mixing of fixed or switched-capacitors and TCR techniques, results in a compensator controlled in generation and absorption modes of operation and having the characteristics of both techniques (Haque and Mali, 1985). Power conversion based static VAR compensators are widely used nowadays in power quality improvement. A statcom is one of such compensators. It is either built using Voltage Source Inverter (VSI) shunted by a DC capacitor or Current Source Inverter (CSI) shunted by a DC reactor (Singh *et al*., 2008; Ye, 2005). Both exchange apparent power with the AC supply through small reactors. They are traditionally governed by angle control scheme which determines the mode of operation and the amounts of phase currents (Tavakoli Bina and Hamill, 2005). Both release harmonics and have real power contribution in the power system network (Filizadeh and Gole, 2005; Chen and Hsu, 2007). Many techniques were approached to minimize these harmonics such as traditional filtering techniques and multilevel technologies in statcom designs (Chen and Hsu, 2007; Hagiwara *et al*., 2012). In this study, a harmonic-free continuously and linearly controlled three-phase inductive static VAR compensator is presented. It is constructed of VSI-base statcom equipped with DC capacitor voltage control. The statcom draws pure inductive phase currents from the AC supply through to some extent small harmonic suppressing rectors. The currents can be varied linearly from zero to maximum value (I_{MAX}) by varying the DC capacitor voltage from its maximum value to its minimum value.

THE PROPOSED COMPENSATOR LAYOUT AND ANALYSIS

The proposed three-phase inductive static VAR compensator is shown in Fig. 1. v_A, v_B and v_C are the three-phase AC supply phase voltages. L and R are the self inductance resistance of the statcom reactors. The voltage source inverter is formed of the IBGT switching devices X_1, X_2, X_3, X_4, X_5 and X_6 which are equipped with the free-wheeling diodes D_1, D_2, D_3, D_4, D_5 and D_6. C_{DC} is the statcom DC capacitor which its voltage is controlled directly by the IGBT S_7. D_7 is a free-wheeling diode for S_7. L_D and R_D are self inductance and resistance of the current limiting reactor for S_7. D_{FW} and C_{FW} are offering free-wheeling path for the current of L_D.

The VSI is triggered by the sinusoidal pulse width modulation shown in Fig. 2. v_{MA}, v_{MB} and v_{MC} are

Corresponding Author: Abdulkareem Mokif Obais, Department of Electrical Power Engineering, Universiti Tenaga Nasional, Malaysia

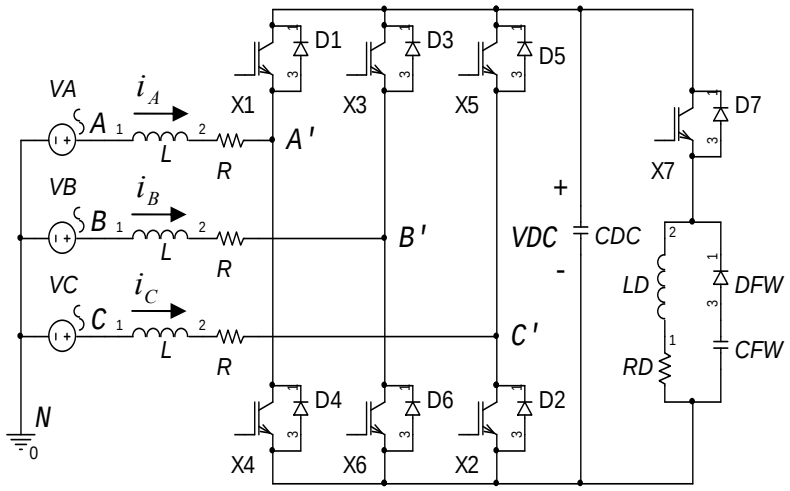

Fig. 1: The proposed three-phase inductive static VAR compensator

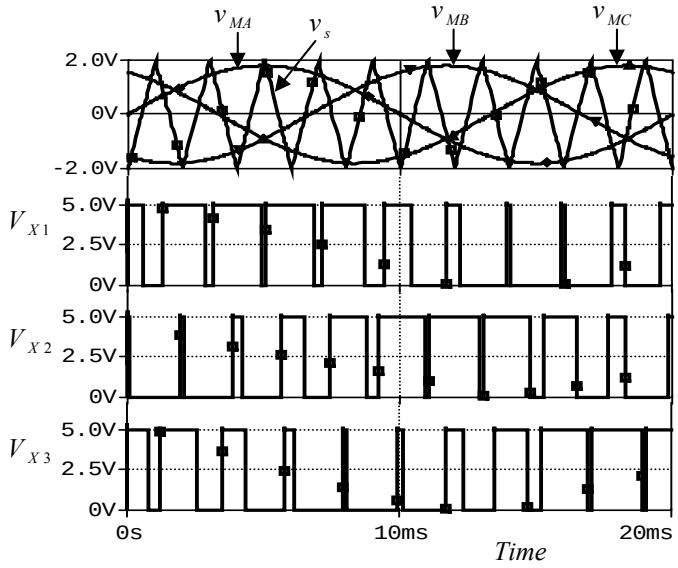

Fig. 2: The voltage source inverter sinusoidal pulse width modulation triggering signals

analogue signals in phase with v_A, v_B and v_C respectively and running with them at the same angular frequency ω. v_{MA}, v_{MB} and v_{MC} are representing the modulating signals and are given by:

$$v_{MA} = kv_A = kV_m \sin \omega t = A_M \sin \omega t \quad (1)$$

$$v_{MB} = kv_B = kV_m \sin\left(\omega t - \frac{2\pi}{3}\right) = A_M \sin\left(\omega t - \frac{2\pi}{3}\right) \quad (2)$$

$$v_{MC} = kv_C = kV_m \sin\left(\omega t - \frac{4\pi}{3}\right) = A_M \sin\left(\omega t - \frac{4\pi}{3}\right) \quad (3)$$

where,

V_m : The amplitude of the phase voltage of the AC power system network

Each of the three modulating signals will be compared with the carrier signal v_S which is a triangular waveform of amplitude of A_S and frequency of f_S. The results of the three comparisons are V_{X1}, V_{X3} and V_{X5} which are representing the triggering signals of the switching devices X_1, X_3 and X_5 respectively. The triggering signals of the switches X_4, X_6 and X_2 are the logic complements of V_{X1}, V_{X3} and V_{X5} respectively. According to the triggering process specified in Fig. 2,

the inverter instantaneous output line voltages $v_{A'B'}$, $v_{B'C'}$ and $v_{C'A'}$ can be given by:

$$v_{A'B'} = \frac{V_{DC}}{5}\left(V_{X1} - V_{X3}\right) \tag{4}$$

$$v_{B'C'} = \frac{V_{DC}}{5}\left(V_{X3} - V_{X5}\right) \tag{5}$$

$$v_{C'A'} = \frac{V_{DC}}{5}\left(V_{X5} - V_{X1}\right) \tag{6}$$

If the carrier signal frequency f_S is very much greater than the modulating signals frequency f which is equal to $\omega/2\pi$, then at any ωt and within one repetition time T_S of the carrier signal cycle, the modulating signals will appear as horizontal straight lines as shown in Fig. 3. Note that the sequence of appearance of these lines depends on ωt. The average values of $v_{A'B'}$, $v_{B'C'}$ and $v_{C'A'}$ within T_S represent the inverter fundamental line voltages at the power system frequency f. In other words, the inverter fundamental line voltages can be given by:

$$\left(v_{A'B'}\right)_F = \frac{1}{T_S}\int_0^{T_S} v_{A'B'}dt' = \frac{1}{T_S}\left(\int_{t'_2}^{t'_3} V_{DC}dt' + \int_{t'_4}^{t'_5} V_{DC}dt'\right) \tag{7}$$
$$= \frac{V_{DC}}{T_S}\left(t'_3 - t'_2 + t'_5 - t'_4\right) = \left(v_{A'}\right)_F - \left(v_{B'}\right)_F$$

$$\left(v_{B'C'}\right)_F = \frac{1}{T_S}\int_0^{T_S} v_{B'C'}dt' = \frac{1}{T_S}\left(\int_{t'_1}^{t'_2} V_{DC}dt' + \int_{t'_5}^{t'_6} V_{DC}dt'\right) \tag{8}$$
$$= \frac{V_{DC}}{T_S}\left(t'_2 - t'_1 + t'_6 - t'_5\right) = \left(v_{B'}\right)_F - \left(v_{C'}\right)_F$$

$$\left(v_{C'A'}\right)_F = \frac{1}{T_S}\int_0^{T_S} v_{C'A'}dt' = \frac{1}{T_S}\left(-\int_{t'_1}^{t'_3} V_{DC}dt' - \int_{t'_4}^{t'_6} V_{DC}dt'\right) \tag{9}$$
$$= \frac{V_{DC}}{T_S}\left(t'_1 - t'_3 + t'_4 - t'_6\right) = \left(v_{C'}\right)_F - \left(v_{A'}\right)_F$$

where, $(v_A)_F$, $(v_B)_F$ and $(v_C)_F$ are the inverter fundamental phase voltages and t'_1, t'_2, t'_3, t'_4, t'_5, t'_6 can be determined from Fig. 3 as follows:

$$t'_1 = \frac{T_S}{4}\left(\frac{v_{MC}}{A_S} + 1\right) = \frac{T_S}{4}\left(m\sin\left(\omega t - \frac{4\pi}{3}\right) + 1\right) \tag{10}$$

$$t'_2 = \frac{T_S}{4}\left(\frac{v_{MB}}{A_S} + 1\right) = \frac{T_S}{4}\left(m\sin\left(\omega t - \frac{2\pi}{3}\right) + 1\right) \tag{11}$$

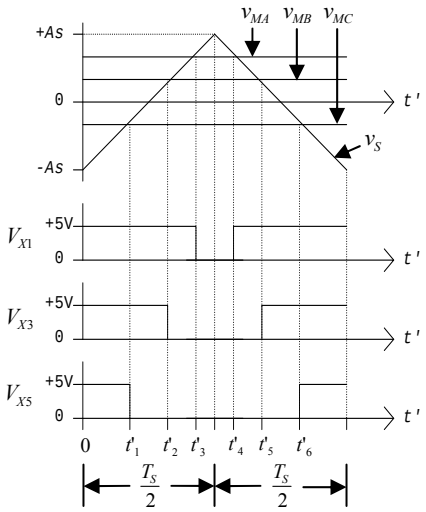

Fig. 3: The voltage source inverter triggering status at certain ωt and within one cycle of v_S

$$t'_3 = \frac{T_S}{4}\left(\frac{v_{MA}}{A_S} + 1\right) = \frac{T_S}{4}\left(m\sin\omega t + 1\right) \tag{12}$$

$$t'_4 = \frac{T_S}{4}\left(3 - \frac{v_{MA}}{A_S}\right) = \frac{T_S}{4}\left(3 - m\sin\omega t\right) \tag{13}$$

$$t'_5 = \frac{T_S}{4}\left(3 - \frac{v_{MB}}{A_S}\right) = \frac{T_S}{4}\left(3 - m\sin\left(\omega t - \frac{2\pi}{3}\right)\right) \tag{14}$$

$$t'_6 = \frac{T_S}{4}\left(3 - \frac{v_{MC}}{A_S}\right) = \frac{T_S}{4}\left(3 - m\sin\left(\omega t - \frac{4\pi}{3}\right)\right) \tag{15}$$

where, m represents the inverter modulation index and is defined by:

$$m = \frac{A_M}{A_S} \tag{16}$$

Substituting for t'_1 to t'_6 in (7), (8) and (9) results in:

$$\left(v_{A'B'}\right)_F = \frac{mV_{DC}}{2}\left(\sin\omega t - \sin\left(\omega t - \frac{2\pi}{3}\right)\right) \tag{17}$$
$$= \frac{\sqrt{3}mV_{DC}}{2}\sin\left(\omega t + \frac{\pi}{6}\right)$$

$$\left(v_{B'C'}\right)_F = \frac{mV_{DC}}{2}\left(\sin\left(\omega t - \frac{2\pi}{3}\right) - \sin\left(\omega t - \frac{4\pi}{3}\right)\right) \tag{18}$$
$$= \frac{\sqrt{3}mV_{DC}}{2}\sin\left(\omega t - \frac{\pi}{2}\right)$$

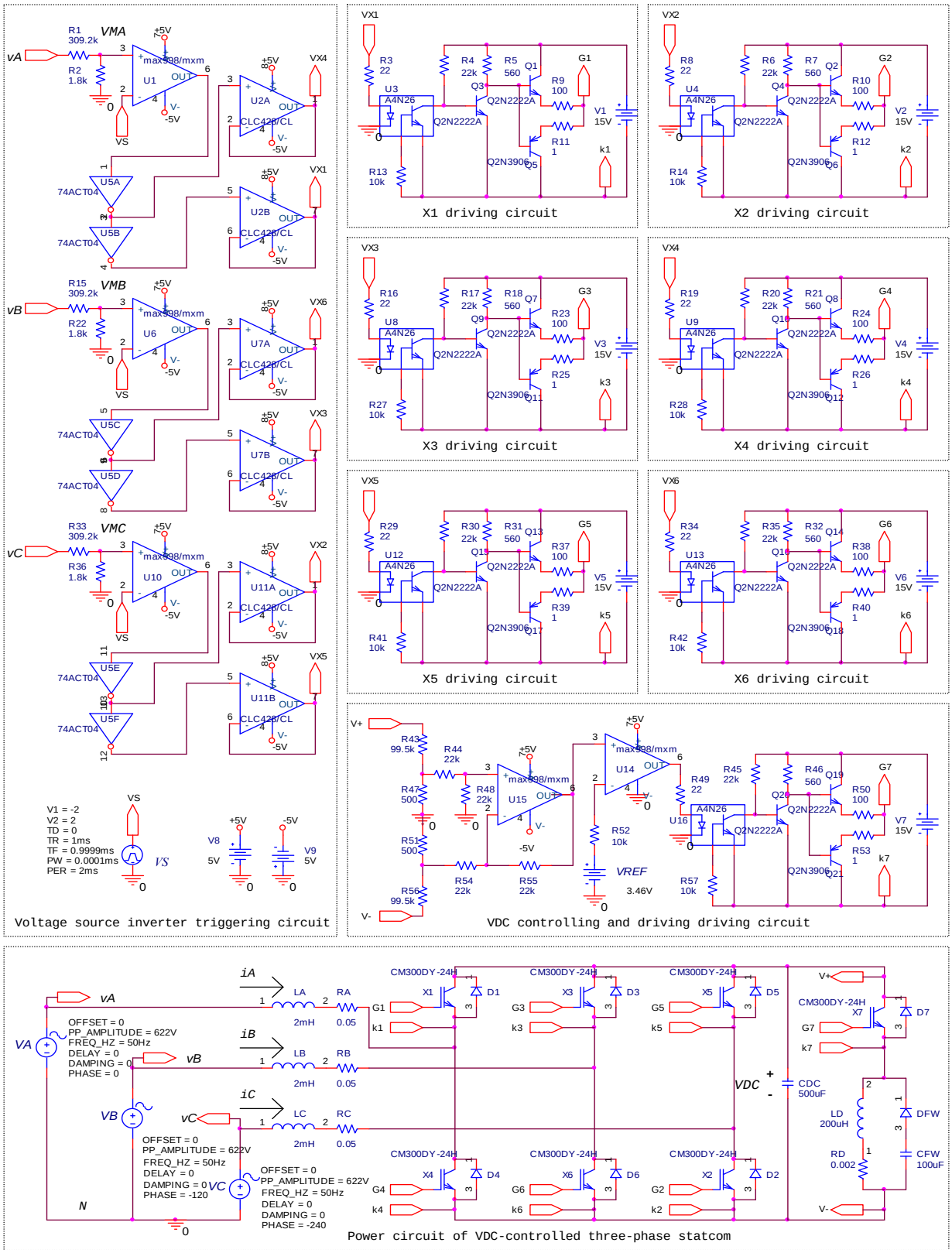

Fig. 4: The PSpice validation system of the proposed compensator

$$(v_{C'A'})_F = \frac{mV_{DC}}{2}\left(\sin\left(\omega t - \frac{4\pi}{3}\right) - \sin(\omega t)\right) \quad (19)$$
$$= \frac{\sqrt{3}mV_{DC}}{2}\sin\left(\omega t - \frac{7\pi}{6}\right)$$

Solving (7), (8), (9), (17), (18) and (19) for $(v_{A'})_F$, $(v_{B'})_F$ and $(v_{C'})_F$ yields:

$$(v_{A'})_F = \frac{mV_{DC}}{2}\sin\omega t \quad (20)$$

$$(v_{B'})_F = \frac{mV_{DC}}{2}\sin\left(\omega t - \frac{2\pi}{3}\right) \quad (21)$$

$$(v_{C'})_F = \frac{mV_{DC}}{2}\sin\left(\omega t - \frac{4\pi}{3}\right) \quad (22)$$

Assuming that $(\omega L)^2$ is very much greater than R^2, V_{DC} is kept constant within its adjusted value and the value of the reactor L is sufficient to suppress all the current harmonics running at the multiples of f_S, then the compensator phase currents will pure reactive and can be given by:

$$i_A = \frac{v_A - (v_{A'})_F}{\omega L} = \frac{1}{\omega L}\left(V_m \sin\omega t - \frac{V_{DC}}{2}\sin\omega t\right) \quad (23)$$

$$i_B = \frac{v_B - (v_{B'})_F}{\omega L} = \frac{1}{\omega L}\left(V_m \sin\left(\omega t - \frac{2\pi}{3}\right) - \frac{V_{DC}}{2}\sin\left(\omega t - \frac{2\pi}{3}\right)\right) \quad (24)$$

$$i_C = \frac{v_C - (v_{C'})_F}{\omega L} = \frac{1}{\omega L}\left(V_m \sin\left(\omega t - \frac{4\pi}{3}\right) - \frac{V_{DC}}{2}\sin\left(\omega t - \frac{4\pi}{3}\right)\right) \quad (25)$$

The DC capacitor voltage V_{DC} is controlled by the switching device S_7. As V_{DC} starts to rise above its adjusted value, S_7 will be turned on causing the capacitor to discharge through the reactor L_D. Once V_{DC} becomes equal to its adjusted value, the discharging process will be terminated.

PSPICE VALIDATION SYSTEM

A complete system of the proposed three-phase statcom-based inductive static VAR compensator using DC capacitor voltage control scheme was designed on PSpice as shown in Fig. 4. In this system a three-phase power system of 380 V, 50 Hz was chosen as the power supply of the proposed compensator. A triangular waveform of frequency f_S of 3.33 KHz was chosen as the carrier signal v_S, thus an inductance of 2 mH for L was sufficient to suppress all current harmonics running at the multiples of f_S. To produce pure reactive phase currents, the reactors self resistance R was chosen such that $R^2 << (\omega L)^2$. The VSI was operated at a modulation index of 0.9. To produce three-phase balanced inductive current in the range of 0 to 200 A (peak values), according to (23), (24) and (25), the capacitor voltage V_{DC} must be controlled linearly in the range of 690V to 400V. I_{MAX} in this compensator is 200A (peak value).

RESULTS AND DISCUSSION

The system of Fig. 4 was tested on PSpice. The results of those tests are shown in Fig. 5, 6, 7 and

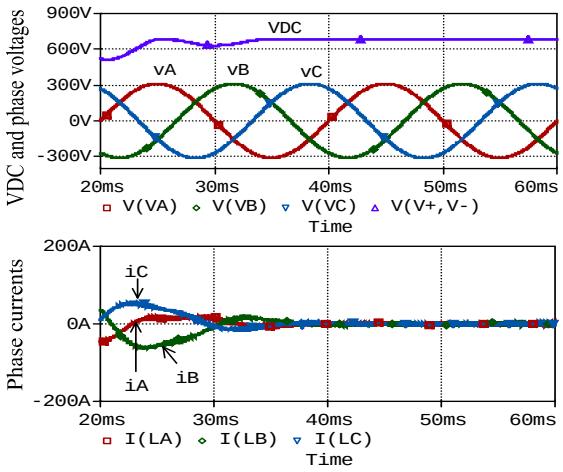

Fig. 5: The compensator phase voltages and currents when $V_{DC} = 690$V

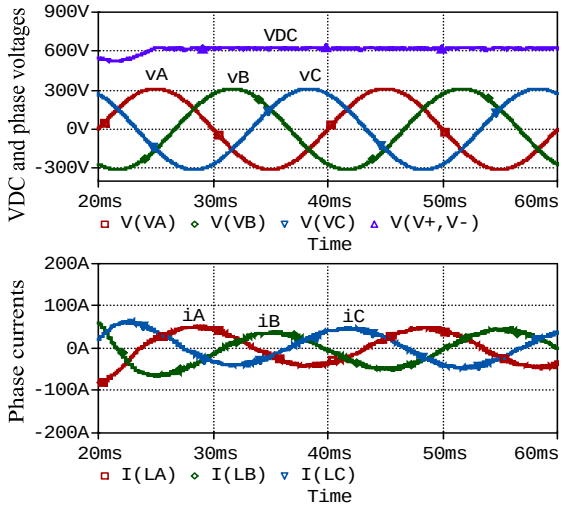

Fig. 6: The compensator phase voltages and currents when $V_{DC} = 610$V

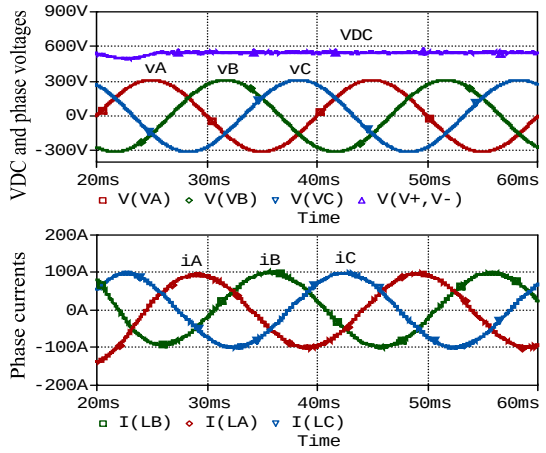

Fig. 7: The compensator phase voltages and currents when $V_{DC} = 540V$

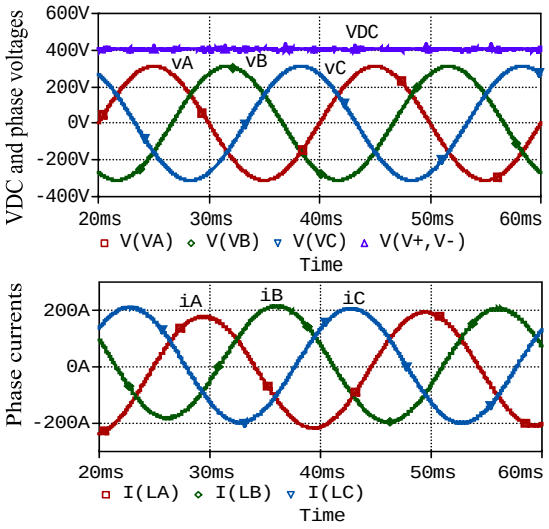

Fig. 8: The compensator phase voltages and currents when $V_{DC} = 400V$

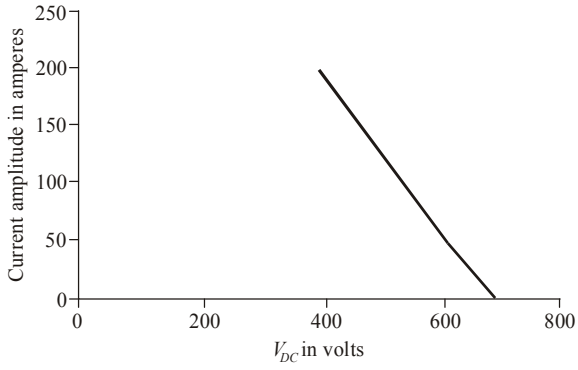

Fig. 9: Phase current amplitude versus V_{DC}

Fig. 8. These figures indicate that the compensator phase currents are pure inductive and having sinusoidal waveforms. The transient time required for these currents to be settled is directly proportional to V_{DC}.

The transient times in Fig. 5, 6, 7 and 8 are due to the times elapsed in charging the capacitor C_{DC}. It is obvious that the compensator phase currents are balanced in phase and magnitudes. The magnitude of these currents was plotted against V_{DC} as shown in Fig. 9. This figure verifies the linearity stated in (23), (24) and (25).

CONCLUSION

The linearity, continuous control, harmonics absence and no real power consumption of the proposed compensator were verified on PSpice which is a computer program representing a reliable replacement of real hardware. The compensator can be used in all applications requiring balanced reactive power absorption. Once the charging time for C_{DC} is elapsed, the compensator will respond rapidly to any change in reactive power demand. Keeping V_{DC} constant within its adjusted value, avoids the compensator to generate current harmonics running at the multiples of the AC supply fundamental frequency *f*.

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