DESIGN OF AN ASYNCRONOUS FREQUENCY MULTIPLIER FOR TWO SINUSOIDAL SIGNALS

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ABSTRACT:

In this paper the conventional frequency multipliers are reviewed and a new technique is adopted. This technique is a multi-stage process which includes sinusoidal to square wave conversion, frequency to d.c voltage conversion, analogue multiplication, magnitude amplification, voltage to frequency conversion, and square wave to sinusoidal wave conversion. The electronic circuit can be easily built and electronic components are commercially available. The whole associated error is less than one percent.

1. INTRODUCTION:

A conventional frequency multiplier may be defined [1] as a device which multiply the input frequency by a factor(n) without losing synchronization with the original waveform (input voltage). It can also be defined as a circuit in which the desired ac output frequency is generally different from the ac input frequency.

Frequency multiplication is widely used in pulse techniques. It is often required to double, triple or multiply the input frequency by a factor n .

Some applications of frequency multipliers are used in communication, Radar, and electronic systems.

Applications of frequency multiplier in Electronics play an important role in our daily life. For example, they help newspapers, networks, local radio and television stations to bring to us the news, and entertainment. Safe secure, and reliable means of electronically communicating voice, image and Computer data have also become essential to the efficient operation of the modern business.

Frequency multipliers are normally constructed using simple varactor or step-recovery diodes. These applications[2] use the distorting effect of nonlinear device to produce harmonics of an input fundamental frequency.

Synchronous frequency multiplier for rectangular-waveforms, based on period-to-voltage conversion [3,4,5,6] are the most common frequency multiplier. The amplification factor of such multipliers can be digitally controlled using digitally controlled potentiometer. Also there are many simple techniques which can achieve doubling, and tripling the frequency of a rectangular waveform.

Phase-locked-loop techniques[7] can also perform frequency multiplication. In such techniques the frequency of the incoming signal (square waveform) can be multiplied by a factor n and the value of n is depending on the voltage controlled oscillator used in the PLL.

There are many techniques applying frequency multiplication on sinusoidal signals. These techniques enable the frequency multiples of cosinusoidal voltage to be generated.

Finally the proposed multiplier is a new one, which achieve frequency multiplication of two sinusoidal signal frequencies. Here the multiplication factor of a certain frequency f1 is another frequency f2 and the output frequency is proportional to f1f2.

2. THE PROPOSED MULTIPLIER SCHEMATIC DIAGRAM:

Conventional multipliers are basically depending on the principle of multiplying a certain frequency by a factor n and hence, they are different from the proposed multiplier whose output is the product of two frequencies f1 and f2 applied at its input terminals. Figure (1) shows the whole multiplier scheme. In the schematic diagram; a mixture of techniques is used. The inputs to the multiplier are two frequencies f1 and f2 and the output is a frequency proportional to the product f1 f2. Note f1, f2, and (f1 f2) represent frequencies of sinusoidal waveforms.

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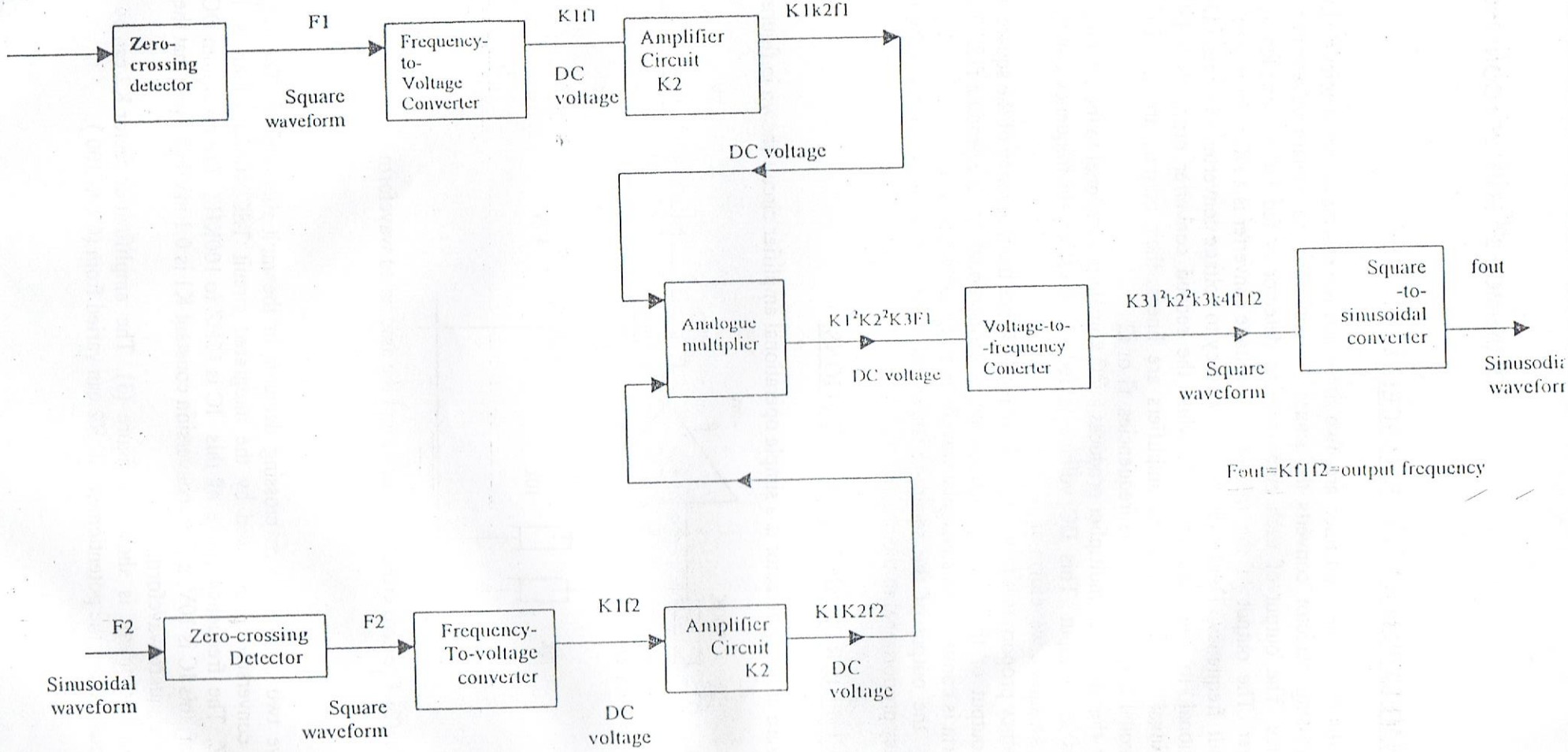


Fig(1) The proposed multiplier schematic diagram.

Note: K1=conversion constant of the frequency to voltage converter, k2= amplification factor of the amplifier, K3=constant of the analogue multiplier,
K4=convertion constant of voltage to frequency converter, and $K=k1^2k2^2k3k4$= the over all constant .

3. THE MULTIPLIER PERFORMANCE:

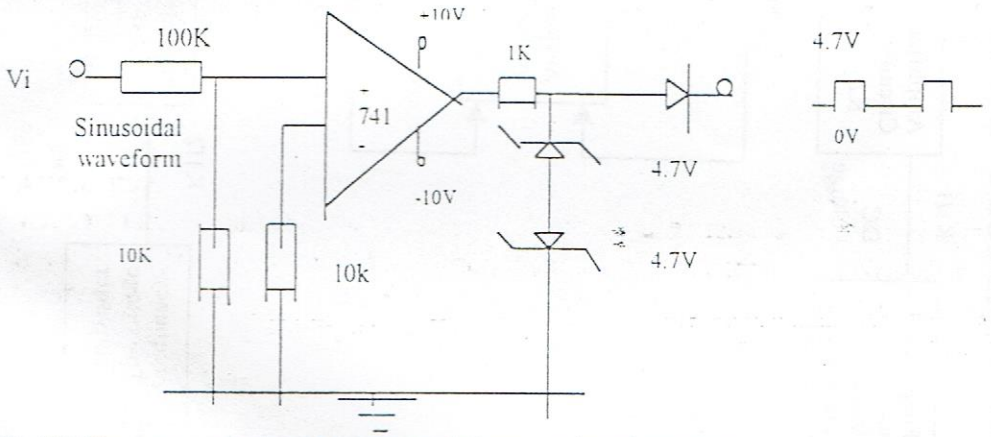
The inputs to the multiplier are two sinusoidal waveforms of frequencies f1 and f2. The zero crossing detector converts the sinusoidal waveform to square waveform at the same frequency. The output of each zero crossing detector is fed into a frequency to voltage converter. The output of the frequency to voltage converter is a DC voltage proportional to the input frequency. Hence the first frequency to voltage converter produces a DC voltage proportional to the frequency f1, while the second converter produces a DC voltage proportional to f2,. Since the amplifiers are linear, their outputs are still DC voltages proportional to their respective frequencies, f1 or f2.

Now the analogue multiplier produces a DC voltage proportional to the product of the DC voltages at its input. This DC voltage is fed to the voltage-to-frequency converter whose output is a square waveform of
a frequency proportional to its DC voltage input, hence the frequency of the square waveform at the output of the voltage-to-frequency is proportional to the product f1f2. This square waveform is converted to sinusoidal waveform at the same frequency.

Finally the output of the square-to-sinusoidal wave converter is a sinusoidal voltage of a frequency proportional to the product f1f2.

4. MULTIPLIER DESIGN SPECIFICATIONS:

The zero crossing detector is a simple operational amplifier circuit shown in figure (2).



Fig(2) The zero crossing detector and the associated waveform.

We have two identical zero crossing detector in the multiplier circuit. The frequency to voltage conversion is achieved by the integrated circuit TSC9400CJ which is linear till 100KHZ. The frequency range of this IC is 10HZ to 100KHZ. The maximum DC voltage output of this IC is 10V, and its conversion constant K1 is 0.1 mV/HZ. Note that the input to this IC is a square waveform.

The amplifier circuit is shown in figure (3). The amplification factor K2 can be adjusted continuously using the potentiometer R. K2 can varied from (0.1 to 100).

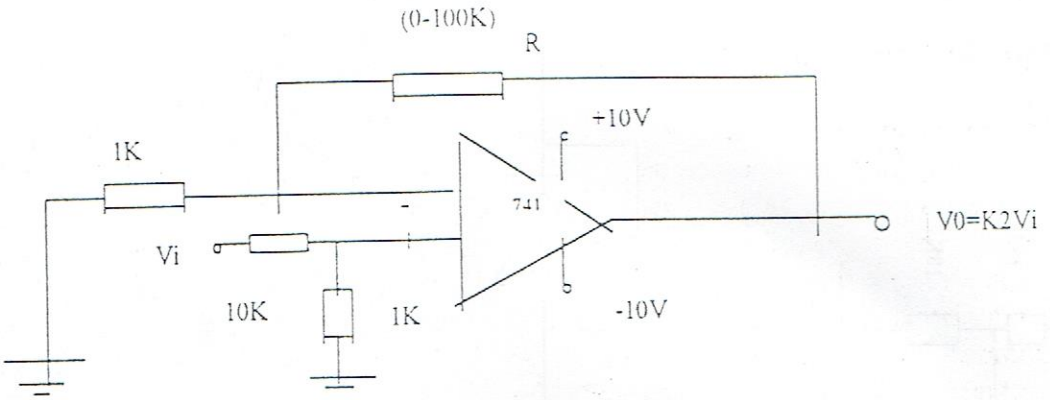
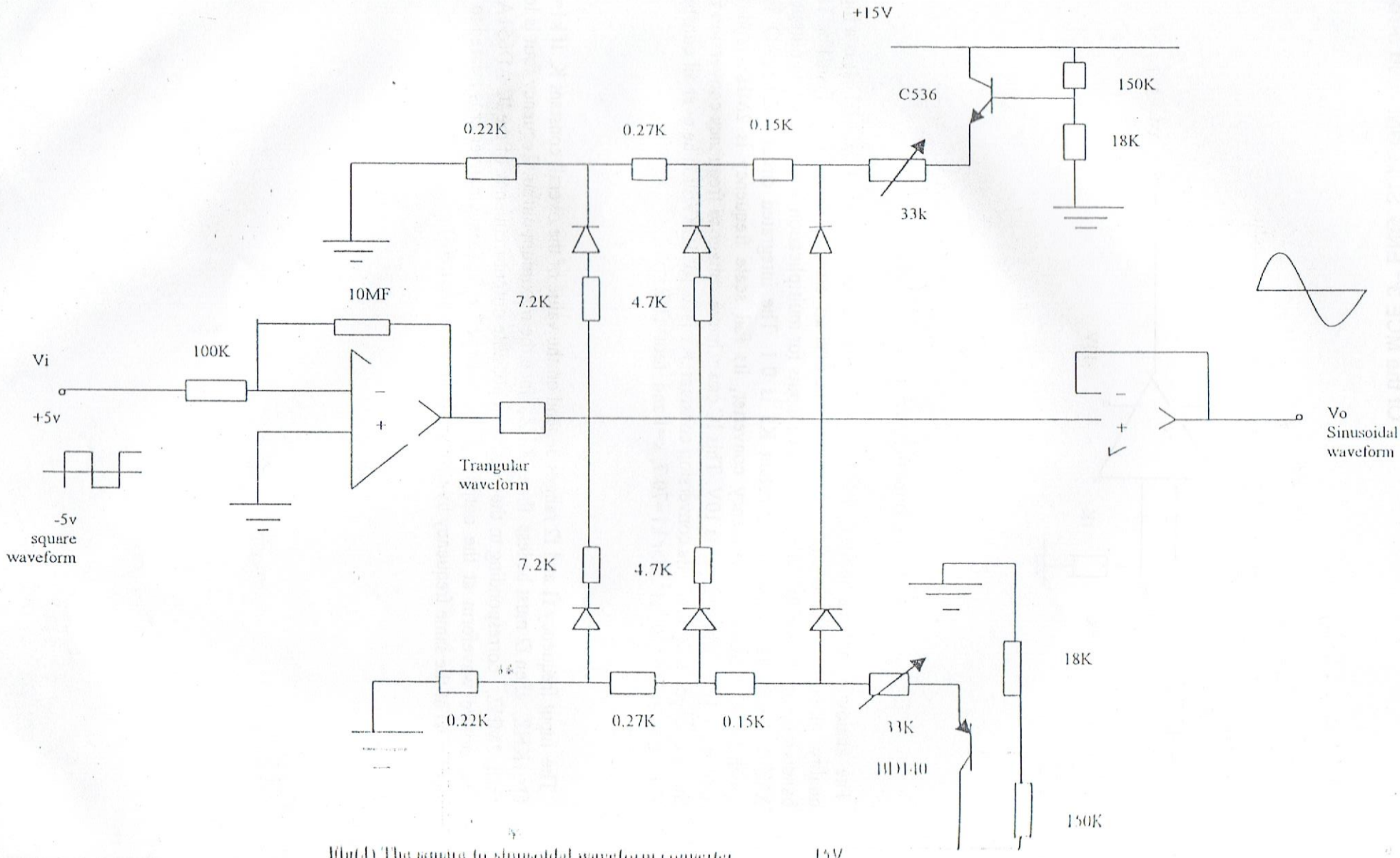


Fig (3) The amplifier circuit

The analogue multiplication is achieved by the integrated circuit AD534JH. It is a high quality monolithic four quadrant multiplier. The over all error of this IC is less than 1%. The bandwidth of this IC is 1MHZ. It has two inputs for multiplication X and Y and its output is XY/10, hence its multiplying constant K3 is 0.1. The integrated circuit AD651AQ is a synchronous voltage to frequency converter, Its full scale frequency is 2MHZ, and its maximum DC voltage input is 10V. This IC can achieve voltage to frequency conversion for the proposed multiplier. Its conversion constant K1 is $2x10^5$ HZ/Volt. The over all constant $k=k1^2k2^2k3k4=2*10^{-4}k1^2$. For k1=70.7, k=1 and fout=f1f2.

The input frequency f1 and f2 ranges depend on the value of the overall constant K. If k1=1, f1=1KHZ, then f2 must be less than 2KHZ, since the maximum output frequency fout is less than 2MHZ, corresponding to the maximum possible output frequency of the IC AD651AQ The square waveform at the output of the voltage to frequency converter is treated to be sinusoidal at the same frequency by the circuit shown in figure(4).



Fig(4) The square to sinusoidal waveform converter

5. CONCLUSION:

This multiplier is an asynchronous one and its output is linear till 2MHZ. The frequency range of the input frequencies f1 and f2 are determined by Themselves and by the limited output frequency fout. It is possible to extend the design to achieve the division of two input frequencies f1 and f2 to obtain an output frequency fout= k f2/f1 or k f1/f2.

6. REFRENCES:

1-Dzunja,Z: An approach to the frequency multiplier analysis, IEEE Transaction on Broadcasting, 1989, VOL.35, NO.1, pp.108-112.

2-PETRO.B.YE: An analysis of steady states of a varactor frequency multiplier with a low-Q input circuit, Radio Eng, and Electron,Phys.1976, VOL.21, NO.6,pp.74-80.

3-Boutin ,N.: A Novel Digital Frequency Multiplier, IEEE 1986, VOL.IM-35, No.4,PP.566-570.

4-Krishnamurthy, K.A. : A simple Frequency Multiplier Int. J. Electronics,1977,VO.43, No.2,pp.201-205.

5-Abdullah,S.A., and Fyath,R.S.: Synchronous Frequency Multiplier for rectangular pulses, Int. J. Electronics, 1986,VOL.60, No.2,pp.239-243.

6-Rao,B.V., and Krishnamurthy,K.A.: A method for frequency multiplication of square waves, Int. J .Electronics, 1976, VOL.40, No.6 , pp.587-592.

7-Orucbilgic: A synchronous frequency multiplier using phase-locked loop, Int. J. Electronics, 1982, VOL.52, No.6, pp. 569-573.

8-Sarafis, G. A., and Karypakas C. A.: Constant gain frequency multiplier, Int. J. Electronics, 1989,VOL.67. No.1, pp.35-41.

9-Cichocki, A.: A sinusoidal frequency multiplying and dividing techniques, Int. J. Electronics, 1983, VOL.54, No.3, pp.427-436.