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A Novel Design Technique of One Stage CMOS OTA For High Frequency Applications

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Abstract – A novel design technique for one stage CMOS Operational Transconductance Amplifier (OTA), based on local common mode feedback circuits is proposed. The idea is to achieve improved gain-bandwidth product (GBW), DC gain, settling time, and slew rate. This is well known that, these parameters are important for high frequency, fast settling applications, such as switched capacitor filters, and analog to digital converters. They have a vast application areas through analog design field, implemented in 0.5µm MIETEC process parameters. The proposed OTA achieves 41.6 MHz (GBW), 67.8dB (DC) gain, 33.7ns settling time and 20.7 V/µs slew rate in ±2.5V supply voltage. The static power consumption is 625µw while driving 15pF load capacitor. Simulation results are included.

Index Term - CMOS OTA Design, Local Common Mode Feedback Circuit, High Frequency Applications.

1. Introduction

High performance A/D converters and switched capacitor filters require OTAs which have both high (DC) gain and a high gain bandwidth product (GBW) [1-2].The advent of deep submicron technologies enable increasingly high speed circuits, but makes designing high (DC) gain OTAs more difficult [3]. A wide variety of analog and mixed signal systems have performance that is limited by the settling time behavior of the CMOS OTAs [4]. The settling time behavior of CMOS OTAs determine the accuracy and speed that can be reduced [5]. Design requirements have been addressed in literature [3-8]. Dynamic biasing of amplifiers has been proposed in [7] as a method for conventional techniques indicates that fast settling requires single pole settling behavior and high gain bandwidth product (GBW)[4,5].These techniques enhance gain and improve settling time. However, in the existing dynamically biased amplifiers, during the last part of settling period the DC gain is very high but the current is very low, thus making settling slowed down [4,5]. Dynamically biased amplifiers have limited acceptance because of these disadvantages [4,5].

Another amplifier design approach proposed for high frequency applications which uses positive feedback techniques to enhance the amplifier (DC) gain without limiting its high frequency performance was proposed by [5,6]. However, most of the existing positive feedback implementations have suffered from problems sighted in references [4,5] such as a strong dependence of amplifier gain on transistor matching [4-6] and the amplifier transfer function which have a denominator of the form$\sum g_o$-g_m [where the g_o^s terms are output conductances of transistors and g_m is transconductance gain of a transistor] has its gate directly connected to the output node of the amplifier [4-6]. Since wide swing operation is generally required, this function will make g_m a strong function of the output signal level. In cascode CMOS OTAs [3], DC gain and gain-bandwidth product are enhanced with the use of extra OTAs. However, this scheme limits the output swing of CMOS OTA and also increase the amplifier input capacitances.

Design techniques proposed in [8] for improvement of gain-bandwidth product and speed of operation requires adaptive biasing circuits which in turn complicate the design and reduce input common -mode voltage range. The design technique proposed in this paper solves the issues mentioned above, and combines excellent performance with simplicity of design. It is suitable for high frequency operation with few modifications on conventional one stage CMOS OTA. It allows not only to avoid limitation on settling time, but also improves small signal characteristics like gain bandwidth product (GBW), DC gain, and slew rate without extra power consumption. A novel design technique of one stage CMOS OTA based on local common mode feedback circuit is proposed. Measurement results for 0.5µm CMOS implementation of these OTAs are included. Their performances are compared to that of conventional one stage CMOS OTA.

2. The Operation of a Conventional One – Stage CMOS OTA

Fig. 1 shows a conventional one stage CMOS OTA. The dc open loop gain , gain bandwidth product, and high impedance pole are

$$A_{OL} = Kg_{m1,2}(r_{o6} // r_{o8}) \tag{1}$$

$$GBW = \frac{Kg_{m1,2}}{2\pi C_L} \tag{2}$$

and $$f_{pout} = \frac{1}{2\pi C_L (r_{o6} // r_{o8})} \tag{3}$$

respectively, where $g_{m1,2}$ is the small-signal transconductance of M_1 and M_2, C_L , $r_{o6}//r_{08}$ are the equivalent capacitance and resistance at the output node, K is the mirror current factor between core stage and shell stage. The internal poles at node A and B are

$$f_{pA,B} = \frac{1}{2\pi C_{A,B} R_{A,B}} = \frac{g_{m3,4}}{2\pi C_{gs3,4}(K+1)} \tag{4}$$

where

$$C_{A,B} \approx C_{gs3,4} + C_{gs5,6} \tag{5}$$

are the parasitic capacitances at nodes A and B, respectively. Typically the condition 2GBW< $f_{pA,B}$ is used in practice to enforce enough phase margin.
The quiescent current flowing through transistors M_1, M_2, M_3, and M_4 and through M_5 and M_6 are $I_{bias}/2$ and $KI_{bias}/2$ respectively. Therefore the maximum current delivered to the load is KI_{bias} and slew rate is therefore, given as

$$SR = \frac{KI_{bias}}{C_L} \tag{6}$$

Or

$$SR = \frac{I_{bias}(2\pi GBW)}{g_{m1,2}} \tag{7}$$

Hence, for a given $C_{L,}$ to avoid limitation of settling time by slew rate K and/or I_{Bias} should be large. An increase in I_{Bias} leads to the same increase in static power dissipation. Larger K values not only increase slew rate, but also GBW and current efficiency [8,9].

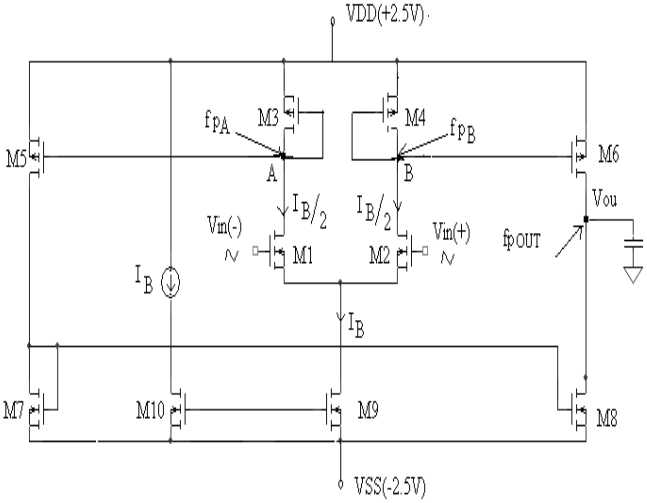

Fig. 1: Circuit Schematic of Conventional One Stage CMOS OTA.

Table 1: Gate dimensions of a conventional one stage CMOS OTA

Transistor number	Aspect ratio (W/L)	Gate width (µm)	Channel length (µm)
M1,M2	12.4	6.2	0.5
M3,M4	4.5	2.2	0.5
M5,M6	13.7	6.8	0.5
M7,M8	4.1	2.0	0.5
M9.M10	6.4	3.2	0.5

3. Design of One Stage CMOS OTA Based On Local Common Mode Feedback Circuit

The proposed one stage CMOS OTA, with local common mode feedback (LCMFB) is shown in Fig. 2

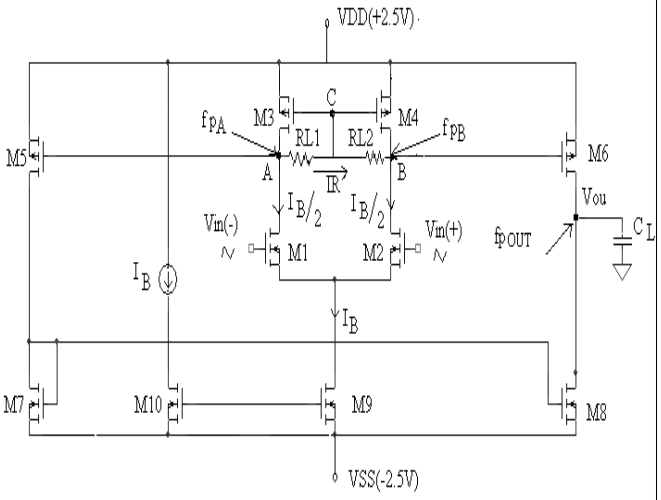

Fig. 2: LCMBF CMOS OTA Using Two Resistors $R_{L1,2}$

Similar to the conventional one stage CMOS OTA, the LCMFB OTA structure utilizes a differential pair (M1,2) and three current mirrors M3,4, M7,8, and M4,6. In the LCMFB circuit however, the active load transistors (M3,4) are reconnected to have a common gate node(C) and matched resistors R_{L1},R_{L2} are used to connect the gate and drain terminals of M3,M4. This simple modification has several performance enhancing benefits versus the conventional OTA architecture including class AB operation which provides enhancement in slew rate (SR), (DC) gain, settling time and gain bandwidth product (GBW), with equal static power dissipation [9]. The analysis of the LCMFB OTA will therefore be based on mirror gain factor with (K=3) and (M1=M2, 3=M4, M5=M6,and M7=M8)[10]. Table 1 presents gate dimensions of a conventional
one stage CMOS OTA.

3.1 Operation of One Stage CMOS OTA With LCMFB

For quiescent (or common mode operation, the drain currents of transistors M1-M8 have equal values ($I_{D1\text{-}8} = I_{bias}/2$) while the current i_R in the resistors R_{L1}, and R_{L2} is zero. The gate-source voltage of M3,4 is the same as their drain source voltage. For common mode signals, these transistors perform as low impedance (diode connected) loads with value

$$R_L^{CM} = \frac{1}{g_{m3,4}} \tag{8}$$

Upon application of a differential signal, the signal current component ($i_d = i_r$) flows through resistors R_{L1},R_{L2}, and are given by[7]:

$$i_{D1,2} = I_D + i_d = \frac{I_{bias}}{2} \pm i_r \tag{9}$$

where

$i_{D1,2}$ is the total drain current, I_D dc biasing current in M1,2, and i_d is the differential current in M1,2 respectively. The drain currents in M3,4 remain unchanged ($i_{D3,4} = I_{bias}/2$). The current i_r generate differential complementary voltage at nodes changes at nodes A, and B while node C remain at a constant voltage. Signal voltages at nodes A, and B are given by: $v_A = -v_B = i_r R_{ML1,2}$ Where V_{SS} is the negative supply voltage as gate voltage of transistors ML1,2, $\beta_{Ml1,2} = K_P(W_{ML1,2}/L_{ML1,2})$, V_C is the constant voltage at node C, and i_r is the signal current in $R_{L1,2}$. This complementary swing at node A,B generates large, non – complementary, signal currents in the shell (M5-M8) of the CMOS OTA by creating large gate source voltage differentials for common source transistors M5,M6, respectively [9].

$$i_r = g_{m1,2}\frac{v_d}{2}\sqrt{1-\left(\frac{v_d/2}{V_{gs1,2}-V_{THN1,2}}\right)^2} \tag{10}$$

where v_d is the applied differential voltage.

3.2 Signal Analysis

Calculation of the open loop gain of the LCMFB CMOS OTA structure requires two independent analyses. The differential input must first be analyzed followed by the common source output shell. The collective LCMFB OTA gain will then be defined as the combination of the previous analyses. The gain will be analyzed focusing on the path from the negative input terminals (at the gate of M1) to the output terminals. This analysis will therefore focus on transistors M1,M3, and M5 but it should be noted that analysis of the positive signal input (at the gate of M2) would yield identical results with equivalent transistor substitution as men tined above.

3.3 Differential Input

Given that the common combined gate of M3,4 (node C) is an AC ground, the circuit can be simplified to the analysis circuit small signal models. The source and gate terminals of M3 are grounded ($v_{gs3} = 0$) in the small signal model eliminating the dependent current source $g_{m3}v_{gs3}$. Thus the small signal current is given by [8-10]: And the equivalent resistance is given by:

$$R_{A,B} = r_{o1,2} // r_{o3,4} // R_{L1,2} \tag{11}$$

$$v_{A,B} = i_{d1,2}R_{out} = (r_{o1,2} // r_{o3,4} // R_{L1,2})(g_{m1,2}v_{gs1,2}) \tag{12}$$

$v_d/2 = v_{gs1,2}$ and the gain of the differential core (A_{CORE}) input stage is given by:

$$A_{CORE} = \frac{v_{A,B}}{v_d} = \frac{g_{m1,2}R_{A,B}}{2} = \frac{(g_{m1,2})(r_{o1,2} // r_{o3,4} // R_{L1,2})}{2} \tag{13}$$

3.4 Common Source Output Shell

The common source output shell consist of common source amplifiers (M5,M6), and current mirror (M7,M8). The output resistance of the LCMFB CMOS OTA is identical to that of the conventional CMOS OTA and is given by:

$$R_{OUT} = r_{o6} // r_{o8} \tag{14}$$

The current mirror has gain (K=3), and the gain of output stage is given by[6] :

$$A_{SHELL} = 2Kg_{m5,6}R_{out} \tag{15}$$

3.5 Collective Open Loop Gain

The open loop gain of the LCMFB CMOS OTA is then given by the multiplication of the input stage ($A_{CORE,}$) and the output shell ($A_{SHELL,}$) as

$$A_{OVL} = Kg_{m1,2}R_{A,B}R_{out} \tag{16}$$

This definition indicates that the (DC) gain of a LCMFB CMOS OTA is a function of programmable resistance $R_{L1,2}$. This dependence provides an interesting characteristics of functionality. For $R_{L1,2} \approx 1/g_m$, $R_{L1,2}$ will dominate the parallel combination $r_{o1,2} // r_{o3,4} // R_{L1,2}$, and the structure will behave as one stage amplifier ($A_{CORE} << A_{SHELL)}$. An increase in $R_{L1,2} \approx r_{o1,2} // r_{o3,4}$ will result in increased gain in the input stage and structure will behave as a two stage amplifier ($A_{CORE} < A_{SHELL}$).

$$PM \approx 90^O - \arctan(\frac{GBW}{f_{A,B}})$$

3.6 AC Analysis

The frequency response of the LCMFB CMOS OTA is determined mainly by the low impedance, high frequency, poles at node A/B, in conjunction with the high impedance, low frequency pole at the output node. The resistance at nodes A/B as a function of the resistances $R_{L1,2}$ [6]:

$$R_{A,B} = r_{o1,2} // r_{o3,4} // R_{L1,2} \quad (17)$$

The parasitic capacitance at A/B is given by:

$$C_{A,B} \approx C_{gs5,6} \quad (18)$$

and the pole at A/B is

$$f_{pA,B} = \frac{1}{2\pi C_{A,B} R_{A,B}} \quad (19)$$

Or

$$f_{pA,B} = \frac{1}{2\pi C_{gs5,6}(r_{o1,2} // r_{o3,4} // R_{L1,2})} \quad (20)$$

3.7 Gain Bandwidth Product (GBW)

The output node capacitance is dominated by the load capacitance and is equal to that of the conventional structure: $C_{OUT} \approx C_L$. The dominant pole/bandwidth of the OTA is also equivalent to the conventional structure and is given by:

$$f_{pout} = \frac{1}{2\pi C_{out} R_{out}} \quad (21)$$

Or

$$f_{p\,out} = \frac{1}{2\pi C_L (r_{o6} // r_{o8})} = f_{3db} \quad (22)$$

equations (16) and (21) are combined for the gain bandwidth product [8]:

$$GBW = \frac{K(g_{m1,2} R_{AB})(g_{m5,6} R_{out})}{2\pi C_L R_{out}} \quad (23)$$

Or

$$GBW = \frac{K(g_{m1,2} g_{m5,6})(r_{o1,2} // r_{o3,4} // R_{L1,2})}{2\pi C_L} \quad (24)$$

The GBW is dependent on the programmable resistance $R_{L1,2}$. As $R_{L1,2}$ increase, the GBW increase.

3.8 Phase Margin PM

The phase margin PM as a function of $R_{L1,2}$ is given by[8]:

$$PM \approx 90^O - \arctan(\frac{GBW}{f_{A,B}}) \quad ^\wedge \quad (25)$$

$$PM \approx 90^o - \arctan\left[K g_{m1,2} g_{m5,6} (R_{L1,2} // r_{O1,2} // r_{O3,4})^2 \frac{C_{gs5,6}}{C_L} \right] \quad (26)$$

This formula allows estimation of the maximum value for $R_{L1,2}$ that can be employed for a given phase margin PM and load capacitance C_L. If $R_{L1,2}$ is too large $\approx r_{o1,2} // r_{o3,4}$ the LCMFB CMOS OTA behaves like a two stage topology and miller compensation is required. Fortunately, it is not necessary to use large values of $R_{L1,2}$ to achieve very high slew rates in our proposed OTA.

3.9 Slew Rate (SR) Of a LCMFB CMOS OTA

The slew rate of LCMFB CMOS OTA is given as

$$SR = \frac{I_{bias}(2\pi GBW)}{g_{m1,2}} \quad (27)$$

Substituting equation (24) in equation (27) we get

$$SR = \frac{K I_{bias}(g_{m5,6}(r_{O1,2} // r_{O3,4} // R_{L1,2})}{C_L} \quad (28)$$

where: $R_{L1,2}$ represent resistors of LCMFB circuit. The last equation indicates that the slew rate of LCMFB CMOS OTA is directly proportional to mirror gain factor and local common mode resistors $R_{L1,2}$.

4. Measurement Results And Performance Comparison of Conventional One-Stage CMOS OTA And LCMFB CMOS OTA

Measurement results by pspice simulation confirm the theoretical calculations, where we summarize the results in table 2, 3, and 4. Table 2 shows that the design of a conventional one stage CMOS OTA is working in high frequencies with acceptable value of DC gain, but these values are not enough for vast application areas.

A novel design of one stage CMOS OTA based on LCMFB circuits has improved performance parameters (eg. GBW, (DC) gain, settling time and slew rate (SR). Simulation results are shown in Fig.4, and summarize in table 3. The results shows that with increase values of common mode resistors $R_{L1,2}$, the GBW, DC gain, slew rate will increased too, but the value of phase margin will decrease so a trade off between phase margin and performance parameters will limit the maximum value of common mode resistors.

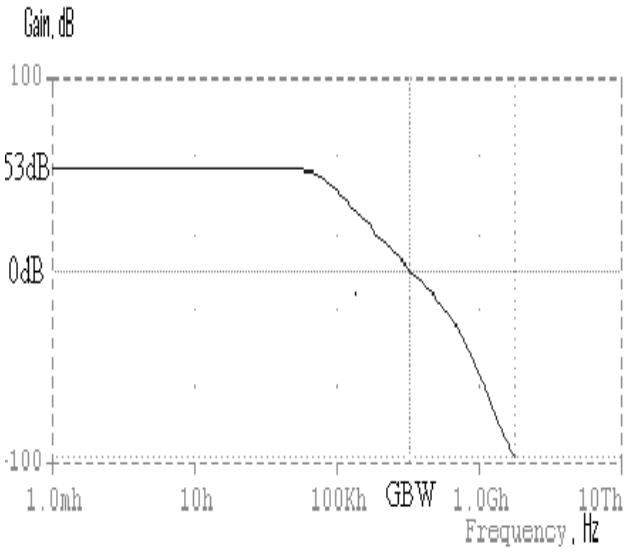

Fig. 3: (a) Frequency Response Magnitude). For The Conventional one stage CMOS OTA

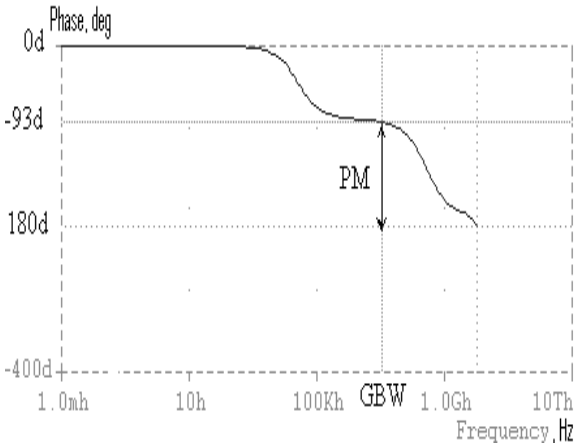

Fig. 3: (b) Frequency response (Phase). For The Conventional One Stage CMOS OTA

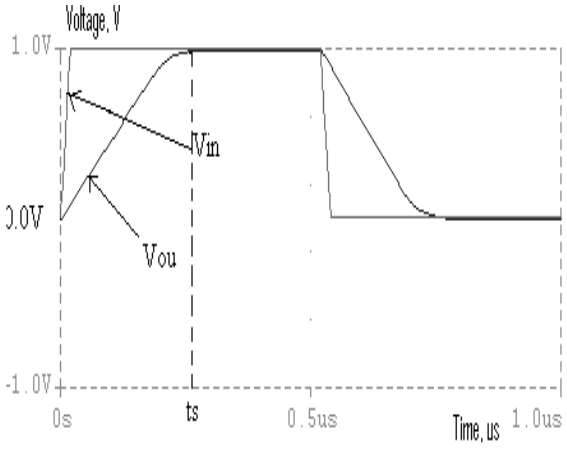

Fig. 3: (c) 1V-Step Transient Response. For The Conventional One Stage CMOS OTA

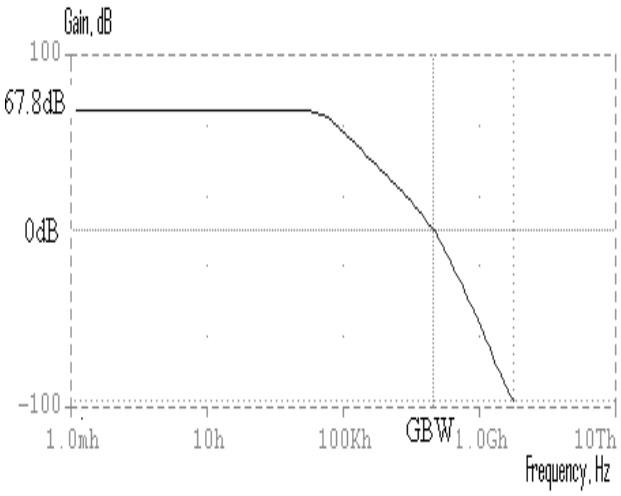

Fig. 4: (a) Frequency Response (Magnitude) For LCMFB CMOS OTA

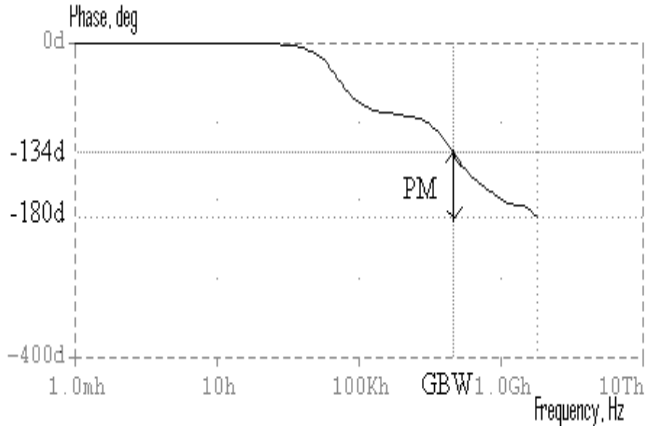

Fig. 4: (b) Frequency Response (Phase) For LCMFB CMOS OTA

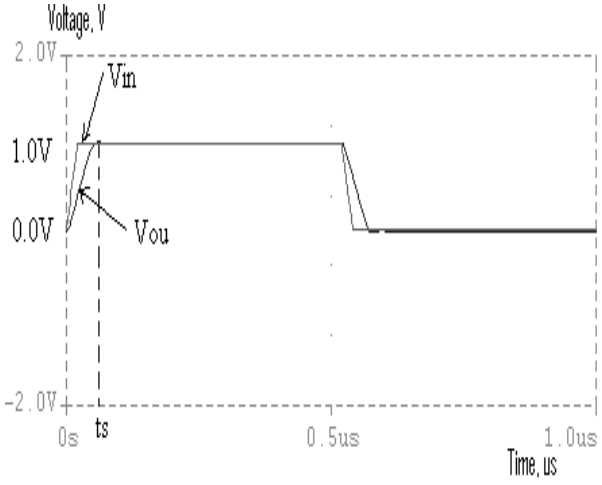

Fig. 4: (c) 1-V Step Transient Response for LCMFB CMOS OTA

Fig. 3 a, b, and c show the frequency response (Magnitude and Phase shift) and 1-V step- transient response of a conventional one stage CMOS OTA. The frequency response shows the unity gain bandwidth of about 11.5MHz with DC gain of 53.0dB, slew rate is 5.3V/μS, and settling time is 200nS. It can be seen that the transient response shows very slow settling time. These parameters is not enough for high frequency applications (eg. Switched capacitor and A/D converter).

Fig. 4 (a), (b), and (c) show the frequency response (Magnitude and Phase shift) and 1-V step- transient response of LCMFB CMOS OTA using two resistors R_{L1} and R_{L2} . The frequency response shows the unity gain bandwidth of 41.6MHz with DC gain of 67.8dB. The transient response shows that the slew rate is 20.7V/uS, and settling time is 33.7ns we note that it is a clear improvement in these performance parameters compared with the conventional CMOS OTA at the cost of reduction in phase margin. Therefore it can be seen that performance parameters of LCMFB CMOS OTA are better compared to conventional CMOS OTA.

Table 2: Summarized results of conventional one stage CMOS OTA

GBW (MHz)	**DC gain (dB)**	**Phase Margin (degree)**	**Slew Rate (V/μS)**	**Settling Time (nS)**
11.5	53.0	87^o	5.7	200

Table 3: Presents GBW, (DC) gain, slew rate (SR), phase margin, and settling time of a LCMFB CMOS OTA, for different values of local common mode resistors RL1,RL2

$R_{L1,2}$ KΩ	**GBW MHz**	**DC Gain dB**	**PM deg.**	**SR V/μS**	**t_S nS**
20	13.0	54.0	87^o	6.4	201.4
40	25.5	60.0	77^O	12.7	101.7
60	34.6	63.6	64^o	17.3	59.2
80	39.1	66.0	54^o	19.5	50.9
100	41.6	67.8	46^o	20.7	33.7
110	44.2	68.6	42^o	22.1	32.5

Table 4: Summarized results of conventional one stage CMOS OTA and one-stage LCMF OTAs

Parameters	**CMOS OTA figure(1)**	**LCMFB CMOS OTA in figure(2)**
(DC) gain	53dB	67.8dB
GBW	11.5MHz	41.6MHz
Phase margin	87^o	46^o
Slew rate	5.7V/μS	20.7 V/μS
Settling time	200ns	33.7ns
Dynamic range	45.4dB	29.8dB
CMRR	55.9dB	55.9dB
$PSRR^+$	81.2dB	66.1dB
$PSRR^-$	52.0dB	50.5dB
Power consumption	625μW	625μW
Die Area	$0.02mm^2$	$0.03mm^2$

5. Conclusions

A novel one stage CMOS OTA based on local common mode feedback circuit, has been designed and compared with a conventional one stage CMOS OTA. The technique employed leads to a significant increase in gain bandwidth product (GBW), (DC) gain , slew rate (SR), and decrease in the settling time without extra power consumption. The design technique proposed in this paper combines better performance with simplicity of design and suitability for high frequency operation with few modifications on conventional one stage CMOS OTA. It allows not only to avoid limitation on settling time, but also to improve small signal characteristics.

These parameters are very important for high frequency, fast settling applications, such as switched capacitor filters, analog to digital converters, and sample and hold circuits. The extra price paid is the decrease in phase margin (PM), but with acceptable values which ensure the stability of the system. Simulation results show good agreement with that of theoretical predictions.

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