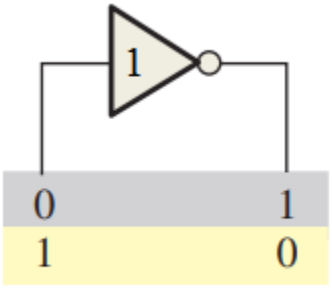
CHAPTER 3
LOGIC GATES

3.1 Logic Gates

Circuits used to process digital signals are called Logic gates. Logic gates operates with binary numbers. All voltages used with Logic gates will be either "High" or "Low". In positive Logic, a High voltage means a binary digits "1", while a Low voltage means a binary digits "0". All digital systems are constructed using these Logic gates. Logic symbols are used to identify these circuits.

3.1.1 NOT (Inverter) gate

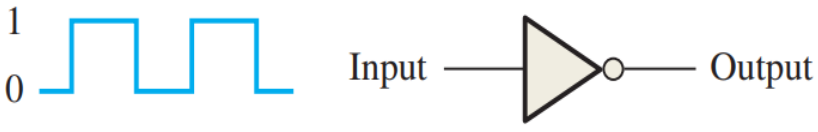
The inverter (NOT circuit) performs the operation called inversion or complementation. The inverter changes one logic level to the opposite level. In terms of bits, it changes a "1" to a "0" and a "0" to a "1".



Inverter

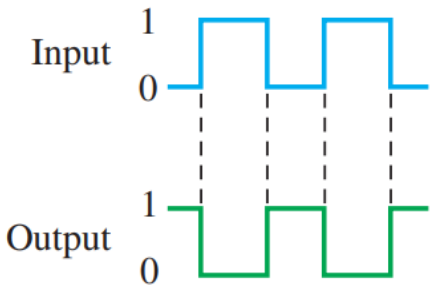
$X = \overline{A}$

Example**:** A waveform is applied to an inverter in following figure. Determine the output waveform corresponding to the input and show the timing diagram. According to the placement of the bubble, what is the active output state?



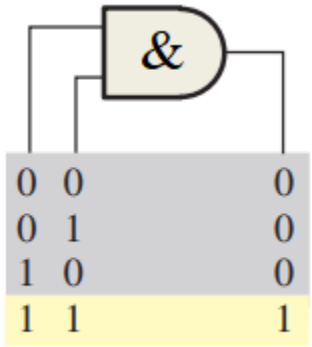
Sol.

The output waveform is exactly opposite to the input (inverted), as shown in following figure, which is the basic timing diagram. The active or asserted output state is 0.



3.1.2 The AND Gate

The AND gate is one of the basic gates that can be combined to form any logic function. An AND gate can have two or more inputs and performs what is known as logical multiplication.



AND

$$X = A \cdot B$$

The total number of possible combinations of binary inputs to a gate is determined by the following formula:

$$N = 2^n$$

Where N is the number of possible input combinations and n is the number of input variables.

Example**:** (a) Develop the truth table for a 3-input AND gate. (b) Determine the total number of possible input combinations for a 4-input AND gate.

Sol.

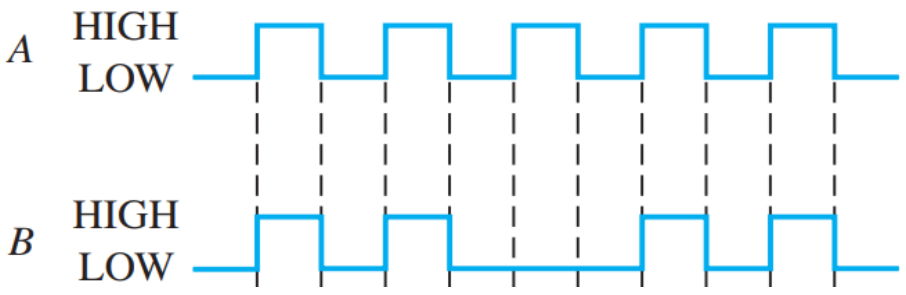
a) There are eight possible input combinations ($2^3 = 8$) for a 3-input AND gate. The input side of the truth table shows all eight combinations of three bits. The output side is all 0s except when all three input bits are 1s.

Truth table for a 3-input AND gate

Inputs			Output
A	***B***	***C***	***X***
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

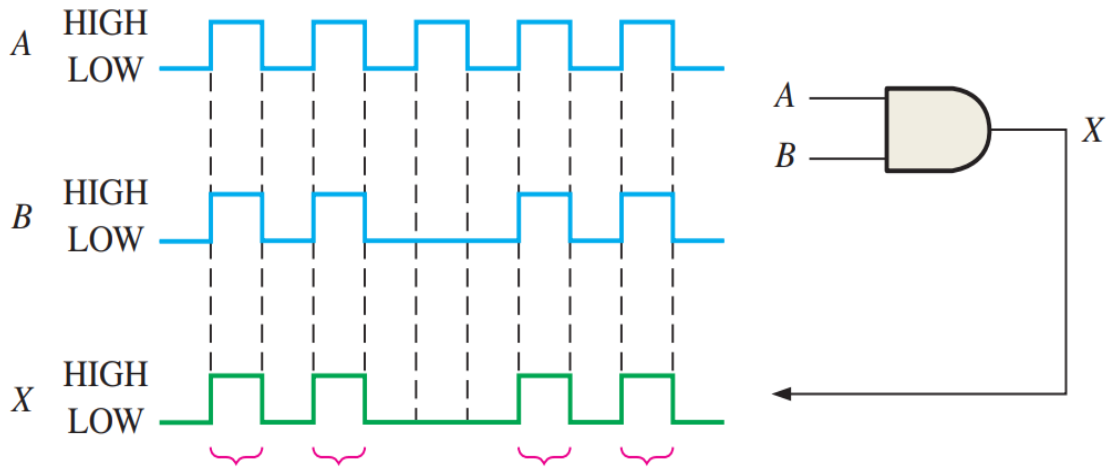
b) $N = 2^4 = 16$. There are 16 possible combinations of input bits for a 4-input AND gate.

Example**:** If two waveforms, A and B, are applied to the AND gate inputs as in following figure, what is the resulting output waveform?



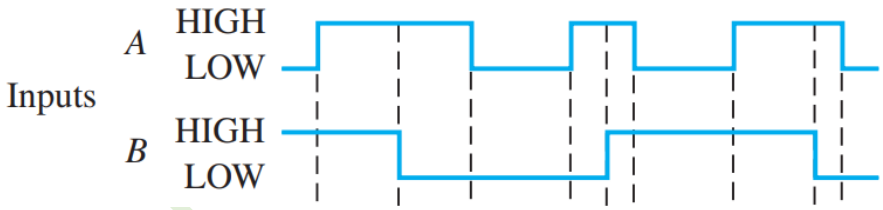
Sol.

The output waveform X is HIGH only when both A and B waveforms are HIGH as shown in the timing diagram.



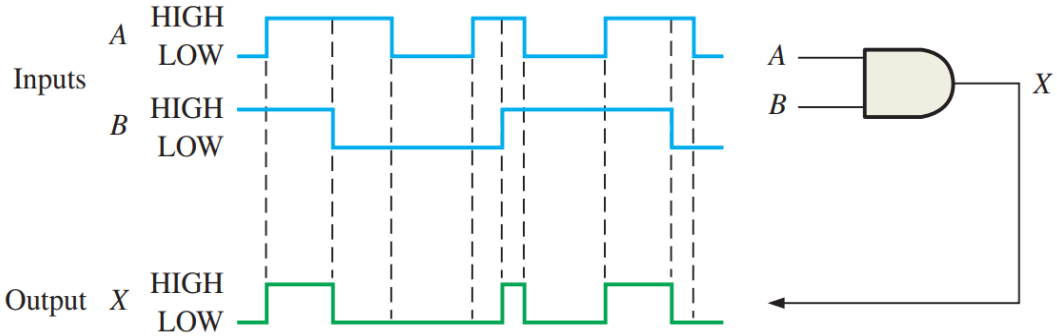
A and B are both HIGH during these four time intervals; therefore, *X* is HIGH

Example**:** For the two input waveforms, A and B, in following figure, show the output waveform with its proper relation to the inputs.



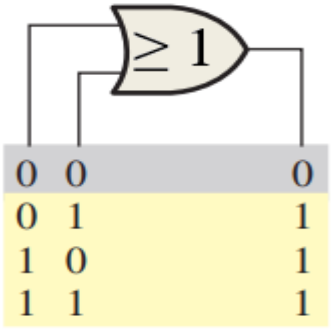
Sol.

The output waveform is HIGH only when both of the input waveforms are HIGH as shown in the timing diagram.



3.1.3 The OR Gate

The OR gate is another of the basic gates from which all logic functions are constructed. An OR gate has two or more inputs and one output, as indicated by the standard logic symbols in Figure below, where OR gates with two inputs are illustrated.

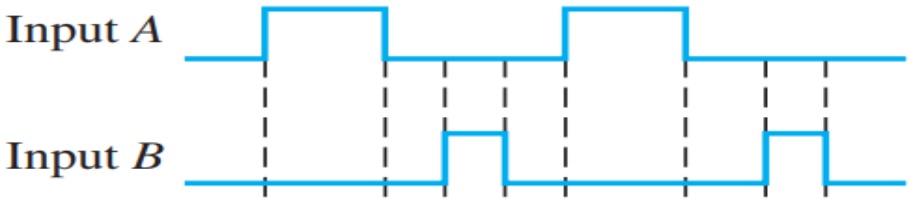


0	0	0
0	1	1
1	0	1
1	1	1

OR

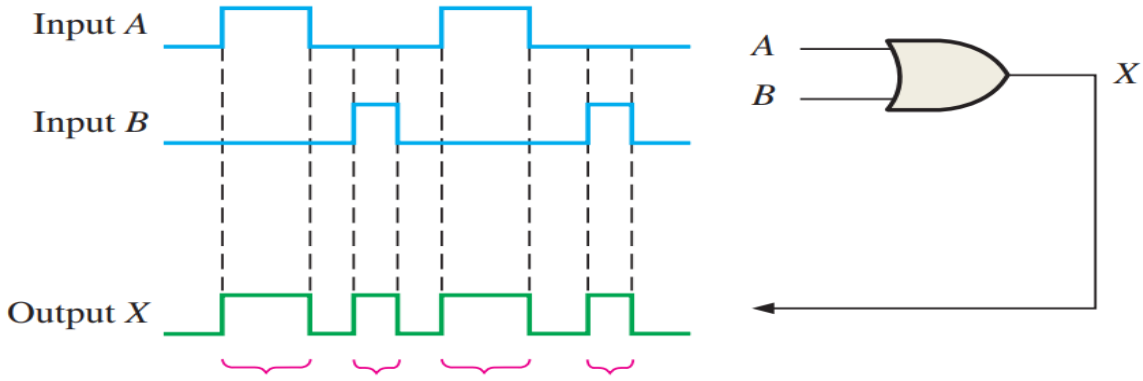
$$X = A + B$$

Example**:** If the two input waveforms, A and B, in following figure are applied to the OR gate, what is the resulting output waveform?



Sol.

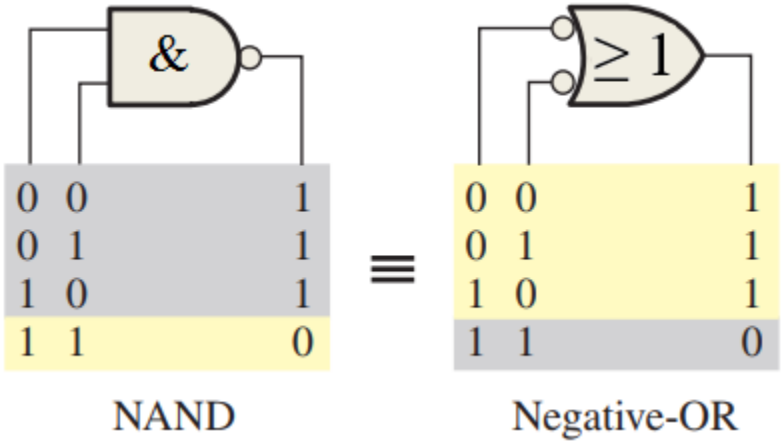
The output waveform X of a 2-input OR gate is HIGH when either or both input waveforms are HIGH as shown in the timing diagram. In this case, both input waveforms are never HIGH at the same time.



When either input or both inputs are HIGH, the output is HIGH

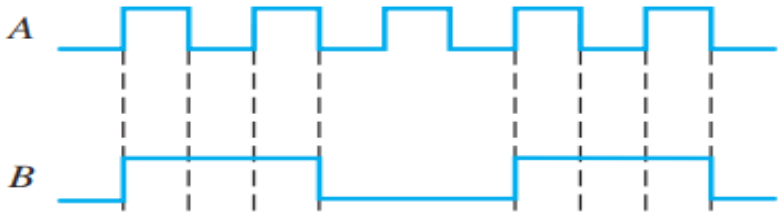
3.1.4 The NAND Gate

The NAND gate is a popular logic element because it can be used as a universal gate; that is, NAND gates can be used in combination to perform the AND, OR, and inverter operations.



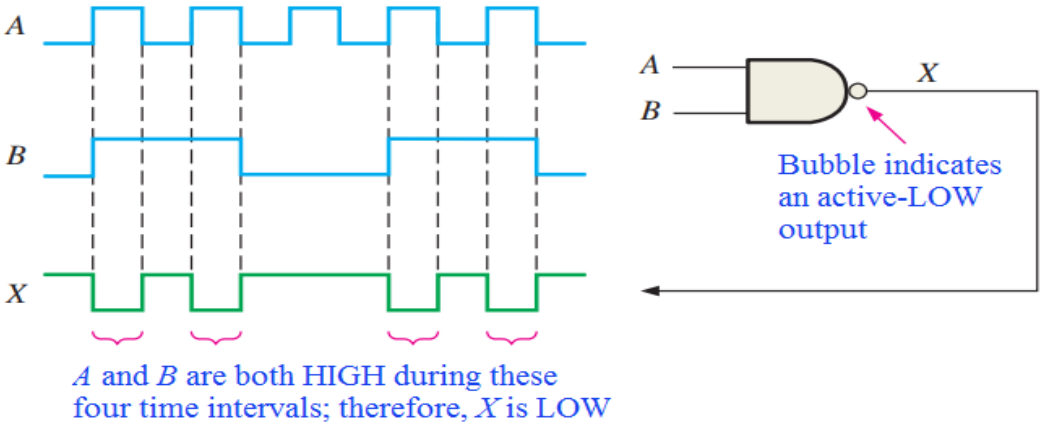
$$X = \overline{A \cdot B}$$

Example**:** If the two waveforms A and B shown in following figure are applied to the NAND gate inputs, determine the resulting output waveform?

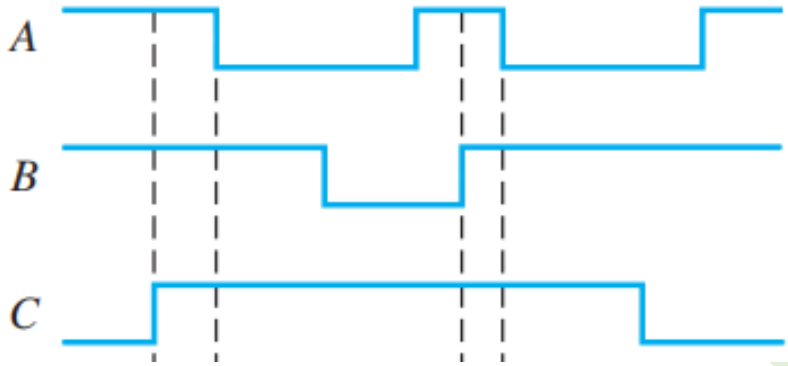


Sol.

Output waveform X is LOW only during the four time intervals when both input waveforms A and B are HIGH as shown in the timing diagram.

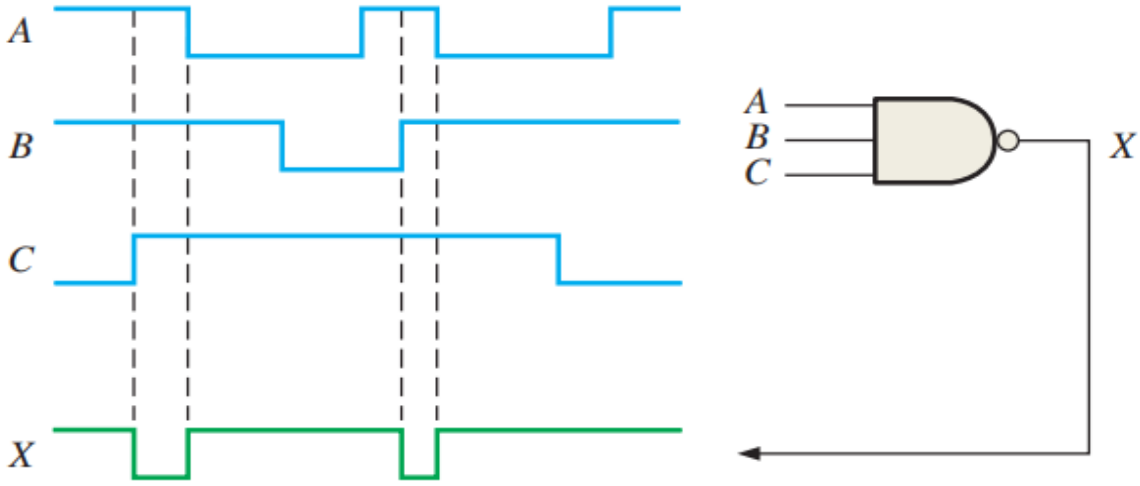


Example**:** Show the output waveform for the 3-input NAND gate in following figure with its proper time relationship to the inputs?

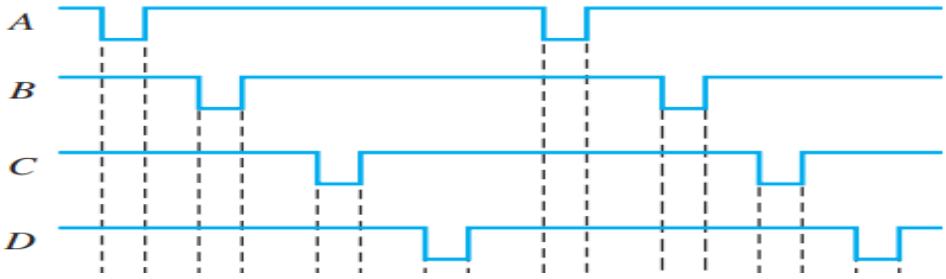


Sol.

The output waveform X is LOW only when all three input waveforms are HIGH as shown in the timing diagram.

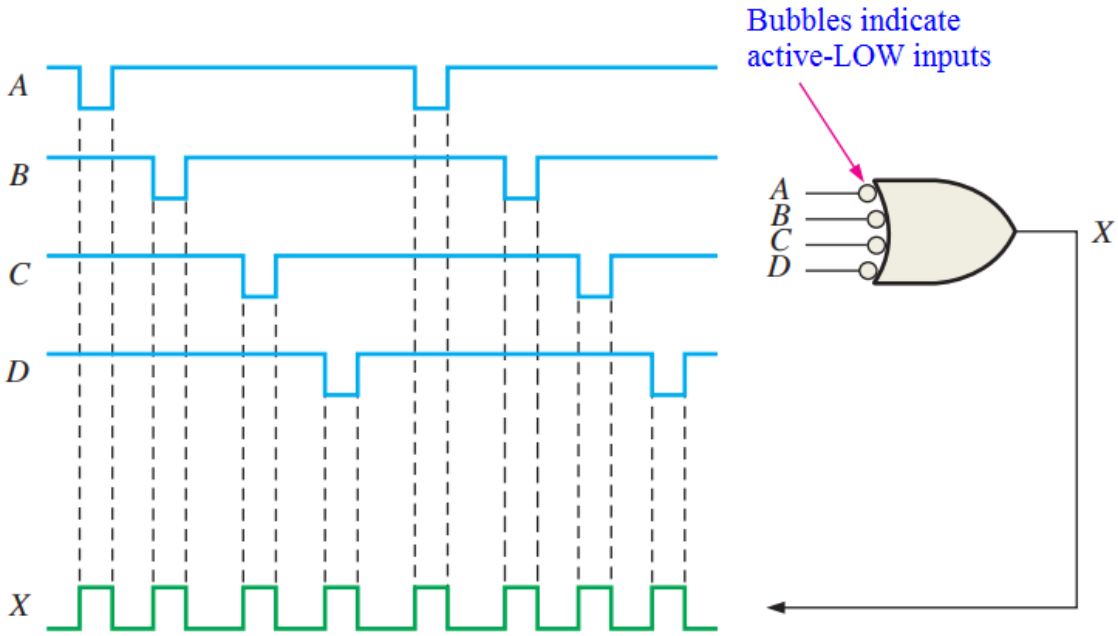


Example**:** For the 4-input NAND gate in the following figure, operating as a negative-OR gate, determine the output with respect to the inputs?



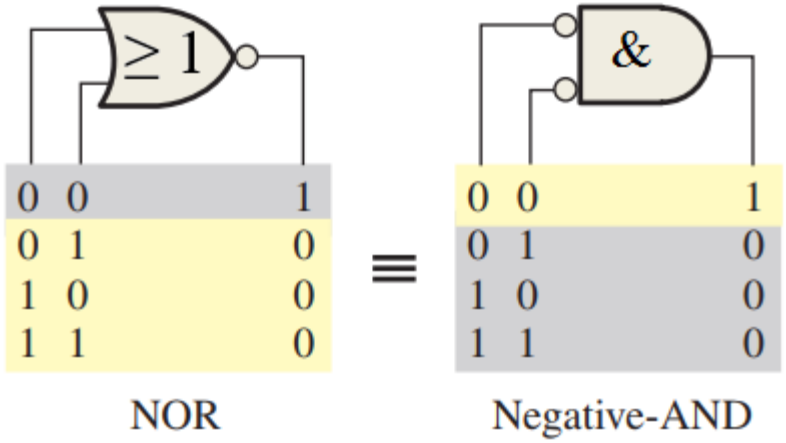
Sol.

The output waveform X is HIGH any time an input waveform is LOW as shown in the timing diagram.



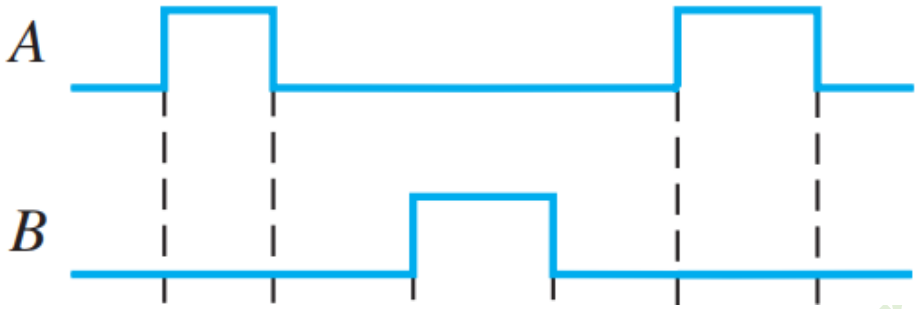
3.1.5 The NOR Gate

The NOR gate, like the NAND gate, is a useful logic element because it can also be used as a universal gate; that is, NOR gates can be used in combination to perform the AND, OR, and inverter operations.



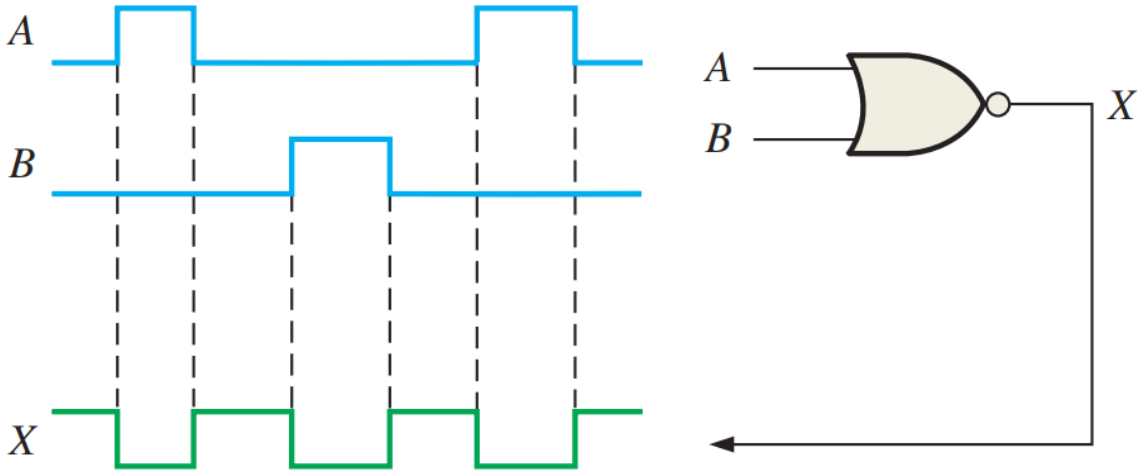
$$X = \overline{A + B}$$

Example: If the two waveforms shown in following figure are applied to a NOR gate, what is the resulting output waveform?

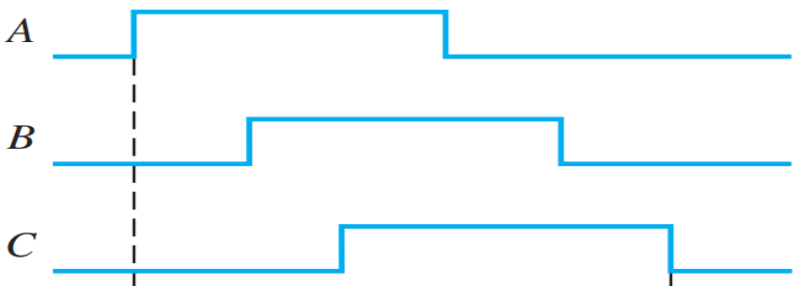


Sol.

Whenever any input of the NOR gate is HIGH, the output is LOW as shown by the output waveform X in the timing diagram.

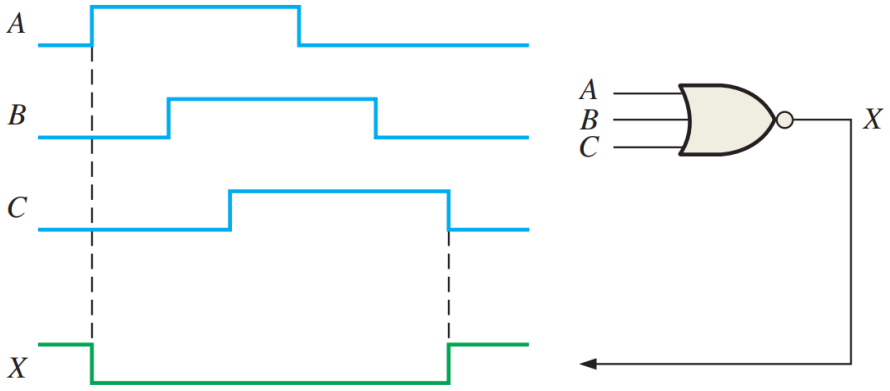


Example: If Show the output waveform for the 3-input NOR gate in following figure with the proper time relation to the inputs?



Sol.

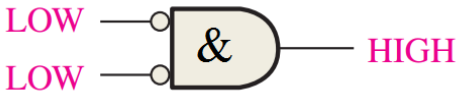
The output X is LOW when any input is HIGH as shown by the output waveform X in the timing diagram.



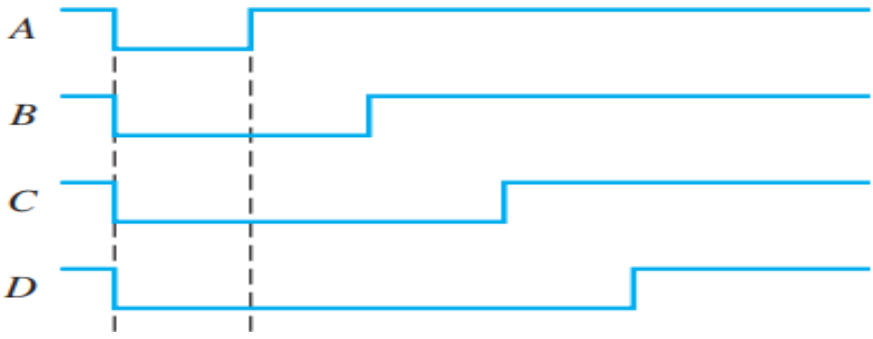
Example: A device is needed to indicate when two LOW levels occur simultaneously on its inputs and to produce a HIGH output as an indication. Specify the device?

Sol.

A 2-input NOR gate operating as a negative-AND gate is required to produce a HIGH output when both inputs are LOW, as shown in following figure

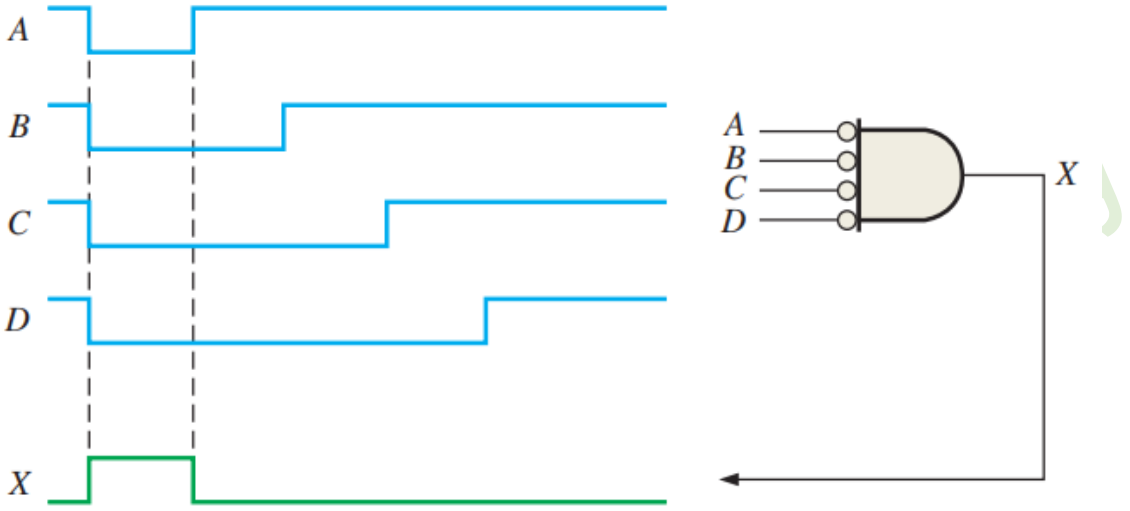


Example: As For the 4-input NOR gate operating as a negative-AND in the following figure, determine the output relative to the inputs?



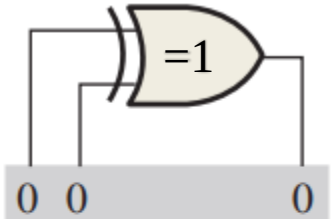
Sol.

Any time all of the input waveforms are LOW, the output is HIGH as shown by output waveform X in the timing diagram.



3.1.6 The Exclusive-OR Gate

The XOR gate has two or more inputs. For two inputs XOR, the output is similar to that from the OR gate except it is "0" when both inputs are "1". In general, an XOR gate gives an output value of "1" when there is an odd number of 1's on the inputs to the gate.



0	0	0
0	1	1
1	0	1
1	1	0

Exclusive-OR

$$X = A \oplus B$$

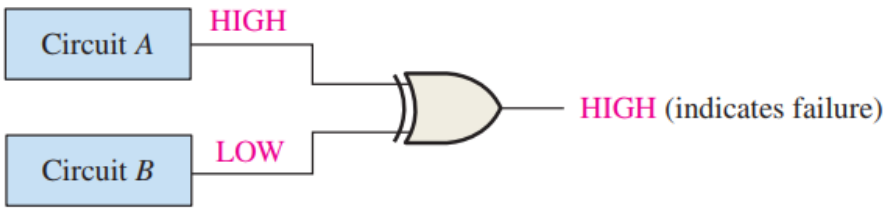
Truth table for a 3-input XOR gate

Input			Output
A	**B**	**C**	**X**
0	**0**	**0**	**0**
0	**0**	**1**	**1**
0	**1**	**0**	**1**
0	**1**	**1**	**0**
1	**0**	**0**	**1**
1	**0**	**1**	**0**
1	**1**	**0**	**0**
1	**1**	**1**	**1**

Example**:** A certain system contains two identical circuits operating in parallel. As long as both are operating properly, the outputs of both circuits are always the same. If one of the circuits fails, the outputs will be at opposite levels at some time. Devise a way to monitor and detect that a failure has occurred in one of the circuits?

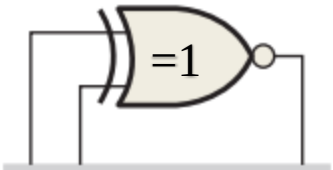
Sol.

The outputs of the circuits are connected to the inputs of an XOR gate as shown in following figure. A failure in either one of the circuits produces differing outputs, which cause the XOR inputs to be at opposite levels. This condition produces a HIGH on the output of the XOR gate, indicating a failure in one of the circuits.



3.1.7 The Exclusive-NOR Gate

The output in this gate is equivalent to inverting the output from the XOR gate. In general, an XNOR gate gives an output value of "1" when there is an even number



0	0	1
0	1	0
1	0	0
1	1	1

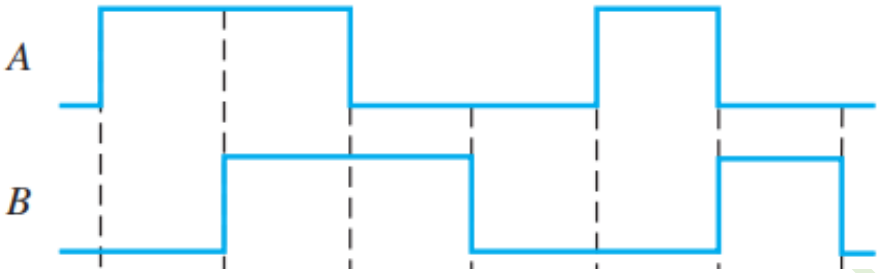
Exclusive-NOR

$$X = A \odot B$$

Truth table for a 3-input NOR gate

Input			Output
A	**B**	**C**	**X**
0	**0**	**0**	**1**
0	**0**	**1**	**0**
0	**1**	**0**	**0**
0	**1**	**1**	**1**
1	**0**	**0**	**0**
1	**0**	**1**	**1**
1	**1**	**0**	**1**
1	**1**	**1**	**0**

Example**:** Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, A and B, in following figure?



Sol.

The output waveforms are shown in previous figure.

Notice that the **XOR** output is HIGH only when both inputs are at opposite levels.

Notice that the **XNOR** output is HIGH only when both inputs are the same.