Solved Examples: Digital Electronics

Ex. 1) *From the following expression fined:*

1. Canonical SOP, POS forms.
2. Standard SOP, POS expressions.
3. The minimal SOP form using K-map.
4. Truth table for the standard SOP, POS expressions.

$$F(A,B,C,D) = (\bar{A}+\bar{B}+\bar{C})\cdot(A+\bar{B})\cdot(A+B+\bar{C})$$

Sol.

1. To find the canonical SOP, POS we must find the missing variables in POS expression:

$\bar{A}$	$\bar{B}$	$\bar{C}$	D	A	$\bar{B}$	C	D	A	B	$\bar{C}$	D
1	1	1	0	0	1	0	0	0	0	1	0
1	1	1	1	0	1	0	1	0	0	1	1
				0	1	1	0				
				0	1	1	1				

Then Canonical **POS** is:

$$F(A,B,C,D) = \prod 2,3,4,5,6,7,14,15$$

Canonical **SOP** is:

$$F(A,B,C,D) = \sum 0,1,8,9,10,11,12,13$$

2. Standard **SOP** is:

$$F(A,B,C,D) = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} + AB\bar{C}\bar{D} + A\bar{B}CD + AB\bar{C}D$$

Standard **POS** is

$$F(A,B,C,D) = (A+B+\bar{C}+D)\cdot(A+B+\bar{C}+\bar{D})\cdot(A+\bar{B}+C+D)\cdot(A+\bar{B}+C+\bar{D})\cdot(A+\bar{B}+\bar{C}+D)\cdot(A+\bar{B}+\bar{C}+\bar{D})\cdot(\bar{A}+\bar{B}+\bar{C}+D)\cdot(\bar{A}+\bar{B}+\bar{C}+\bar{D})$$

Solved Examples: Digital Electronics

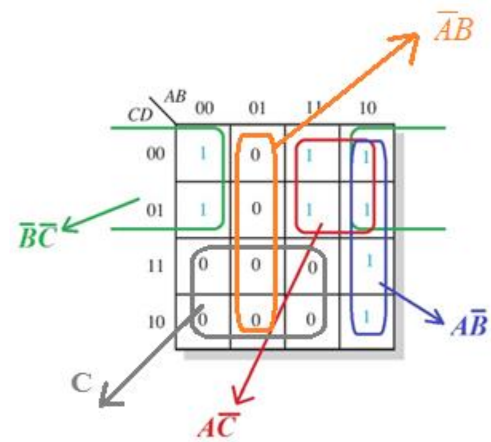
3. Minimal expression using K-map:

Min SOP: $F(A,B,C,D) = A\bar{B} + A\bar{C} + \bar{B}\bar{C}$

Min POS: $\bar{F}(A,B,C,D) = C + \bar{A}B$

$F(A,B,C,D) = \overline{C + \bar{A}B}$

$F(A,B,C,D) = (C).(A + \bar{B})$



4. Truth table for standard **SOP,POS** expressions:

Inputs				**Output**
A	**B**	**C**	**D**	**F**
0	**0**	**0**	**0**	**1**
0	**0**	**0**	**1**	**1**
0	**0**	**1**	**0**	**0**
0	**0**	**1**	**1**	**0**
0	**1**	**0**	**0**	**0**
0	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**0**	**1**	**1**
1	**0**	**1**	**0**	**1**
1	**0**	**1**	**1**	**1**
1	**1**	**0**	**0**	**1**
1	**1**	**0**	**1**	**1**
1	**1**	**1**	**0**	**0**
1	**1**	**1**	**1**	**0**

Solved Examples: Digital Electronics

Ex. 2) If the **7-bit hamming code** word received by a receiver is (**1011000**). Assuming the even parity state whether the received code word is correct or wrong. If wrong locate the bit having error?

Sol.

P_1	P_2	d_1	P_3	d_2	d_3	d_4
1	0	1	1	0	0	0

$$A = P_1 \oplus d_1 \oplus d_2 \oplus d_4 = 1 \oplus 1 \oplus 0 \oplus 0 = 0$$

$$B = P_2 \oplus d_1 \oplus d_3 \oplus d_4 = 0 \oplus 1 \oplus 0 \oplus 0 = 1$$

$$C = P_3 \oplus d_2 \oplus d_3 \oplus d_4 = 1 \oplus 0 \oplus 0 \oplus 0 = 1$$

CBA = $(110)_2 = (6)_{10}$

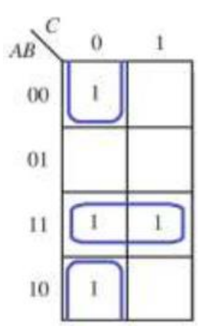
The error is found in the 6^{th} bit (i.e. d_1)

The correct message is (1011010)

Ex. 3) *Determine the simplify expression by the truth table below using Karnaugh map method*?

Sol.

$$F(A,B,C) = AB + \overline{B}\overline{C}$$

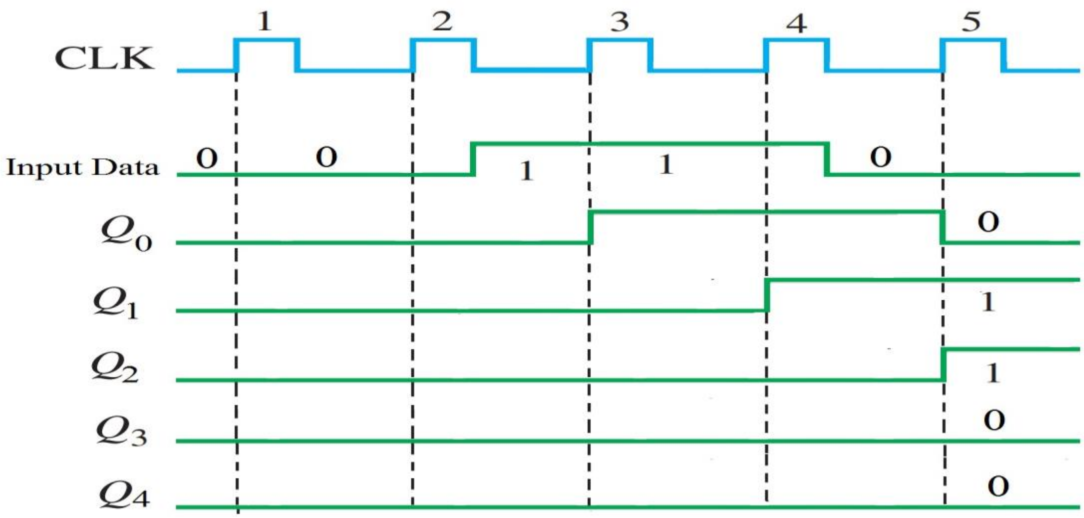


A	*B*	*C*	*F*
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Solved Examples: Digital Electronics

Ex. 4) Draw the waveform to shift the number **00110** into the **SISO** shift register (built from **DF.F.**). Assume the register is initially cleared **(all 0's)**?

Sol.



Ex.5)

***Simplify the following expressions using the rules of Boolean algebra*:**

1. $Z(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{C}$

Sol.

$$Z(A,B,C) = \bar{A}\bar{B}(\bar{C} + C) + \bar{A}\bar{C}$$

$$Z(A,B,C) = \bar{A}\bar{B} + \bar{A}\bar{C} = \bar{A}(\bar{B} + \bar{C})$$

$$Z(A,B,C) = \bar{A}(\overline{B \cdot C}) = \overline{A + BC}$$

2. $F(A,B,C,D) = (A\bar{B}(C + BD) + \bar{A}\bar{B})C$

Sol.

$$F(A,B,C,D) = (A\bar{B}C + \bar{A}\bar{B})C \;=\; A\bar{B}C + \bar{A}\bar{B}C$$

$$= \bar{B}C(A + \bar{A}) = \bar{B}C$$

Solved Examples: Digital Electronics

3. $\boldsymbol{Y(A,B,C) = A[B + C(AB + AC)]}$

Sol.

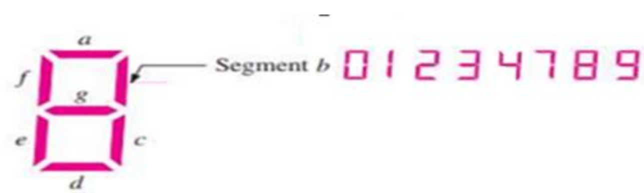
$$\boldsymbol{Y(A,B,C) = A[B + ABC + AC]}$$

$$\boldsymbol{Y(A,B,C) = A[B(1 + AC) + AC]}$$

$$\boldsymbol{Y(A,B,C) = A(B + AC)}$$

$$\boldsymbol{Y(A,B,C) = AB + AC = A(B + C)}$$

1. **Ex.6)** In a 7-segment display, segment-b is activated for the digits 0, 1, 2, 3, 4, 7, 8, 9, as illustrated in the figure below. Since each digit can be represented by a BCD code, derive an SOP expression for segment-b using the variables ABCD and then minimize the expression using a K - map.

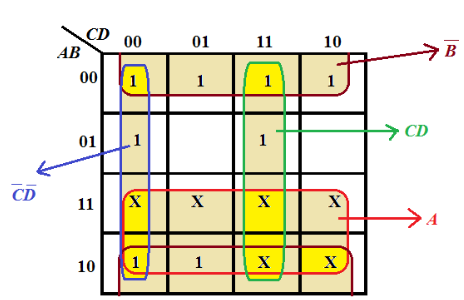


Sol.

The expression for segment-b is:

$$b = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$$

Each term in the expression represents one of the digits in which segment-b is used. The Karnaugh map minimization is shown in the figure below. X's (don't care) are entered for those states that do not occur in the BCD code.



Solved Examples: Digital Electronics

From the K - map, the minimized expression for segment-b is:

$$F(A,B,C,D) = A + \bar{B} + CD + \bar{C}\bar{D}$$

Ex. 7) Design a synchronous counter that can count numbers **(0, 4, 1, 3, 2, 7, 6, and 5)** and repeat using **T Flip Flop**?

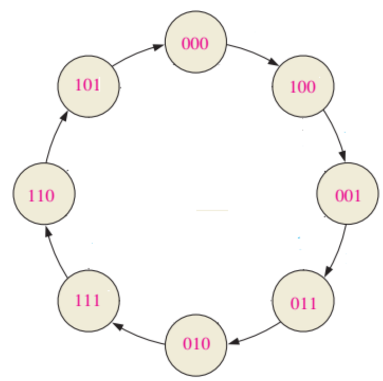
Sol.

No. of state = N $=2^n = 2^3 = 8$

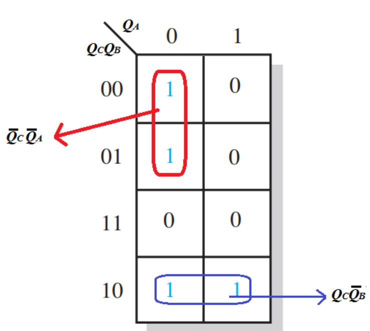
Max. of count = N-1 = 8-1 = 7

State diagram

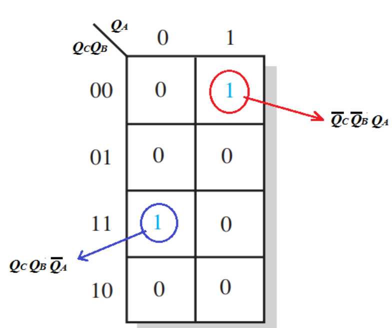
Present state			Next state			Input of F.F		
Q_C	**Q_B**	**Q_A**	**Q_C**	**Q_B**	**Q_A**	**T_C**	**T_B**	**T_A**
0	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**
0	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**1**
0	**1**	**0**	**1**	**1**	**1**	**1**	**0**	**1**
1	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
1	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**
1	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**1**



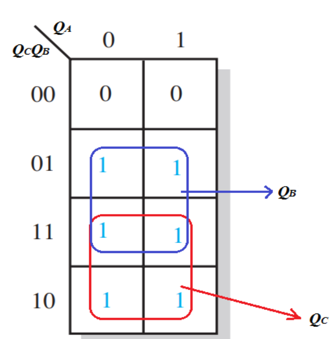
F.F. input expressions using K-map



$T_C = Q_C\,\bar{Q}_B + \bar{Q}_C\,\bar{Q}_A$



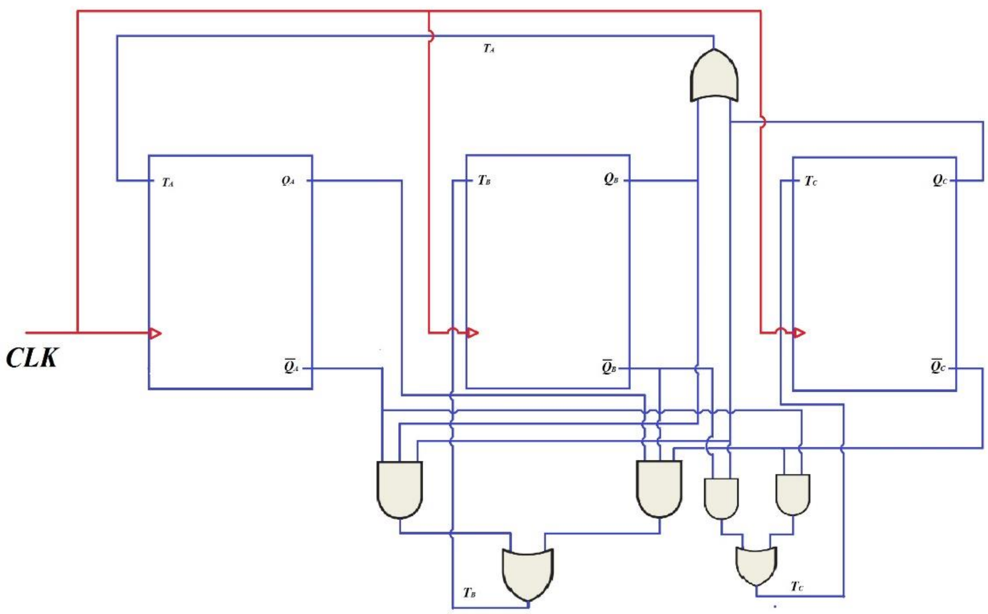
$T_B = Q_C\,Q_B\,\bar{Q}_A + \bar{Q}_C\,\bar{Q}_B\,Q_A$



$T_A = Q_C + Q_B$

Solved Examples: Digital Electronics

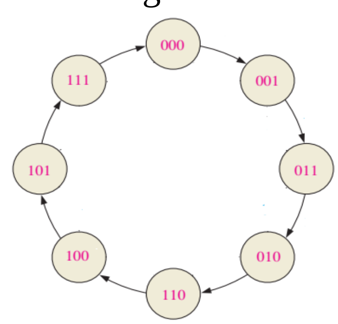
Logic circuit designed



Ex. 8) Design a synchronous counter that can count numbers **(0, 1, 3, 2, 6, 4, 5, and 7)** and repeat using **JK Flip Flops**?

Sol.

State diagram



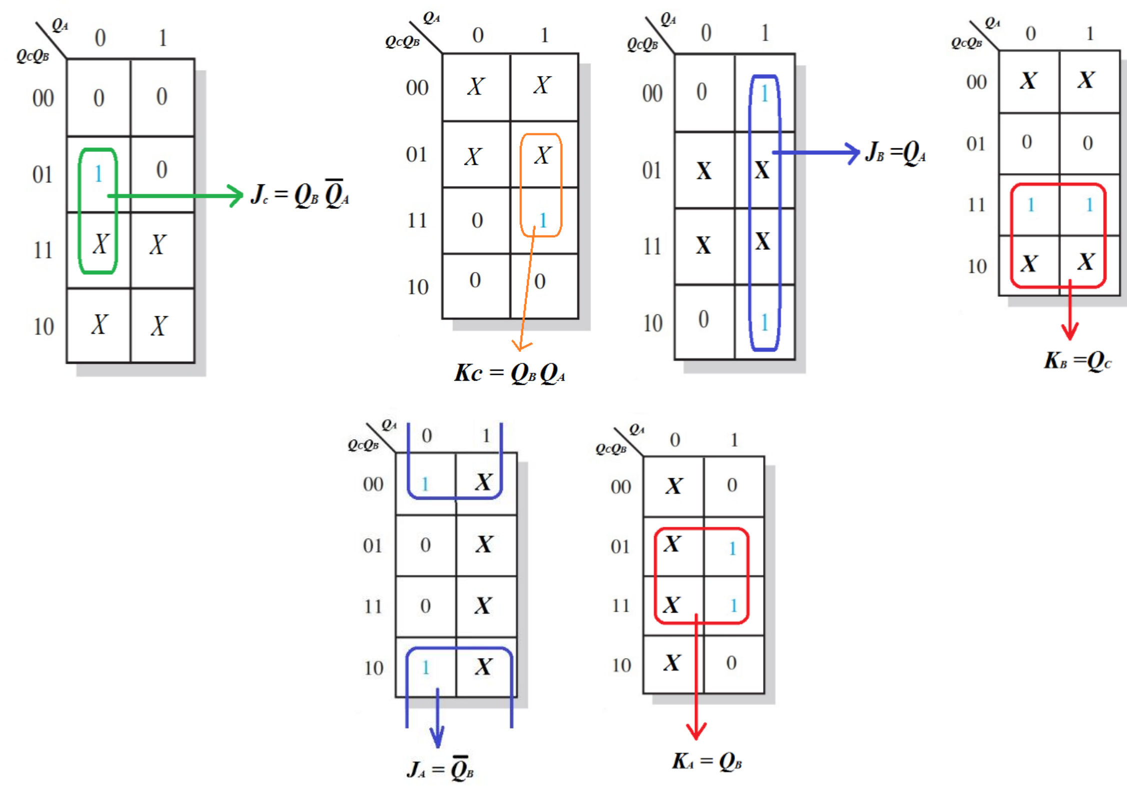
No. of state = N $=2^n=2^3=8$

Max. of count = N-1 = 8-1 = 7

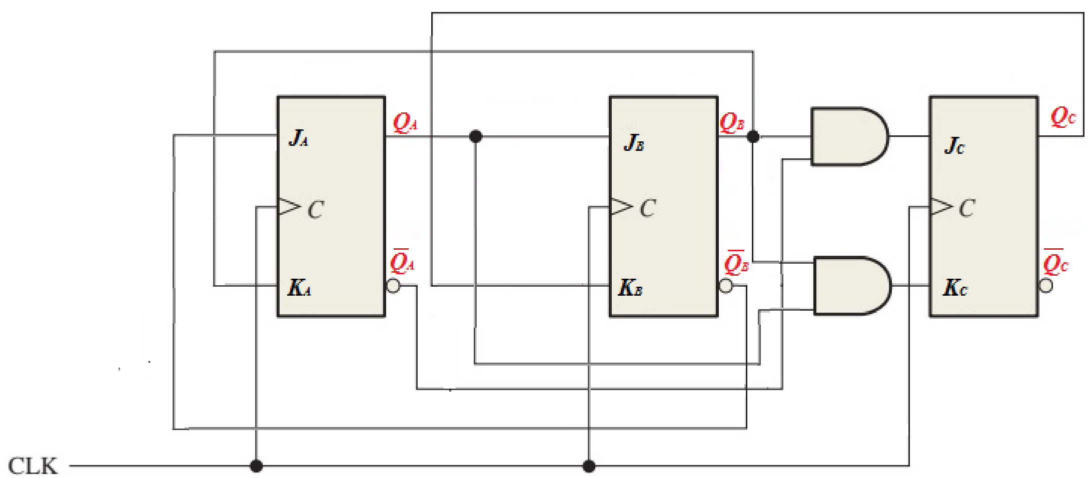
Present state			Next state			Input of F.F.					
Q_C	Q_B	Q_A	Q_C	Q_B	Q_A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	1	1	0	1	X	X	0	0	X
1	1	0	1	0	0	X	0	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	1	X	0	1	X	X	0
1	1	1	0	0	0	X	1	X	1	X	1

Solved Examples: Digital Electronics

F.F. input expressions using K-map

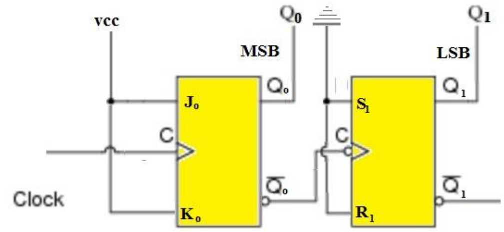


Counter circuit diagram

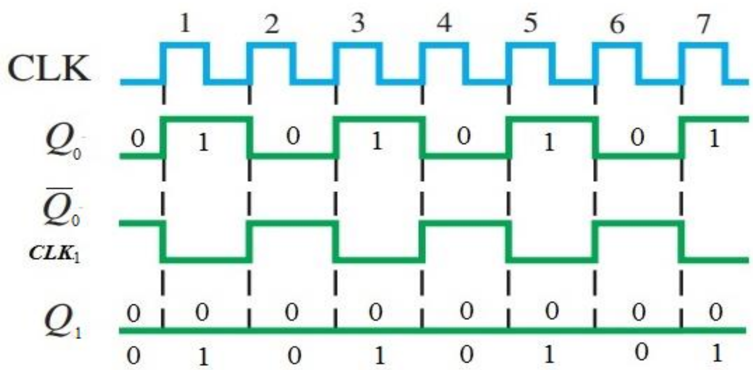


Solved Examples: Digital Electronics

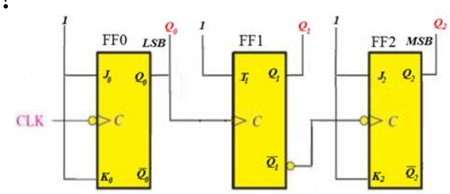
Ex. 9) For an asynchronous counter in figure below, draw the timing diagram for **(6 Clock)** and find which numbers this counter can count. Begin with counter cleared?

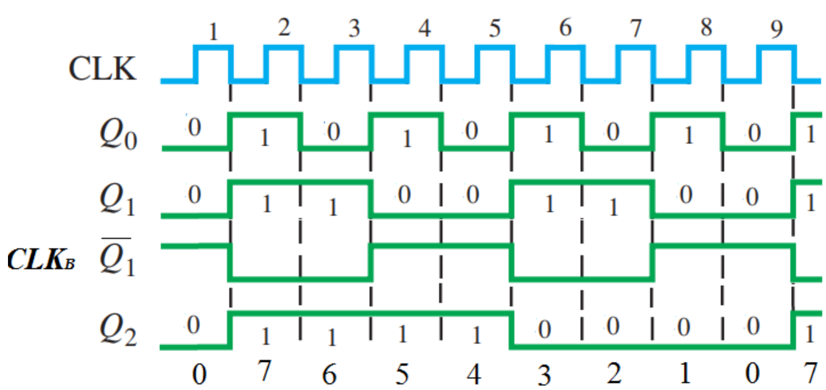


Sol.



Ex. 10) For an asynchronous counter in figure below, draw the timing diagram for **(9 Clock)** and find which numbers this counter can count. Begin with counter cleared?





Solved Examples: Digital Electronics

Ex.11) *From the following expression fined:*

1. Canonical POS form.
2. Standard SOP, POS expressions.
3. The minimal SOP, POS forms using K-map.
4. Truth table for the standard SOP, POS expressions.

$F(A,B,C,D) = \sum(0,1,2,5,8,9,10)$

Sol.

1. Canonical **POS** is:

$$F(A,B,C,D) = \prod 3,4,6,7,11,12,13,14,15$$

2. Standard **SOP** is:

$$F(A,B,C,D) = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + A\bar{B}C\bar{D}$$

Standard **POS** is

$$F(A,B,C,D) = (A+B+\bar{C}+\bar{D})\cdot(A+\bar{B}+C+D)\cdot(A+\bar{B}+\bar{C}+D)\cdot(A+\bar{B}+\bar{C}+\bar{D})\cdot(\bar{A}+B+\bar{C}+\bar{D})\cdot(\bar{A}+\bar{B}+C+D)\cdot(\bar{A}+\bar{B}+C+\bar{D})\cdot(\bar{A}+\bar{B}+\bar{C}+D)\cdot(\bar{A}+\bar{B}+\bar{C}+\bar{D})$$

3. Minimal expression using K-map:

Min. **SOP**:

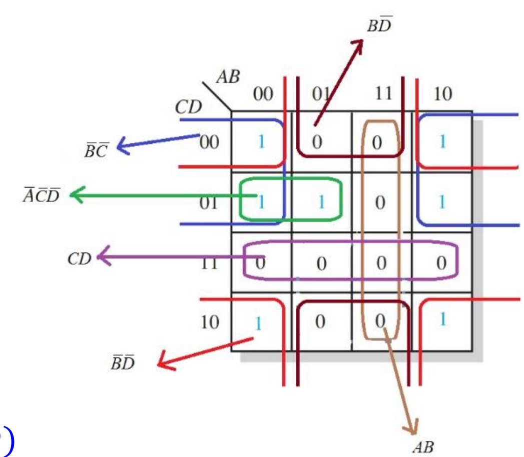
$$F(A,B,C,D) = \bar{B}\bar{C} + \bar{A}\bar{C}D + \bar{B}\bar{D}$$

Min. **POS**:

$$\bar{F}(A,B,C,D) = AB + CD + B\bar{D}$$

$$F(A,B,C,D) = \overline{(AB + CD + B\bar{D})}$$

$$F(A,B,C,D) = (\bar{A}+\bar{B})(\bar{C}+\bar{D})(\bar{B}+D)$$



Solved Examples: Digital Electronics

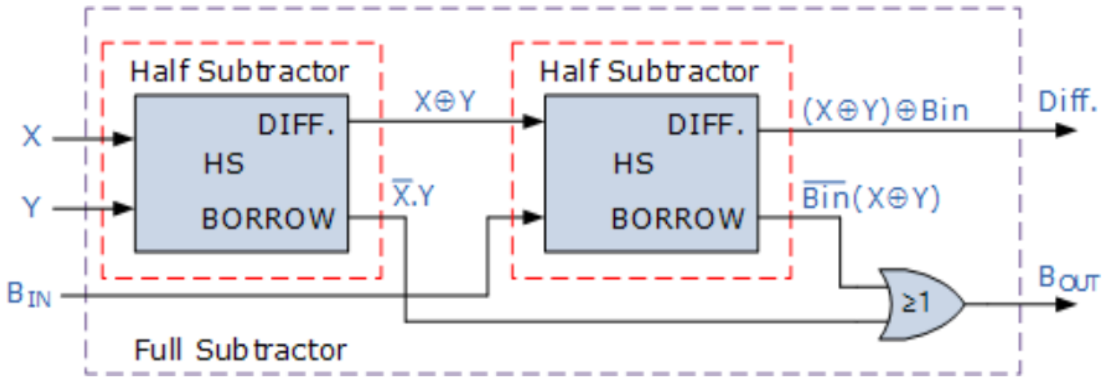
4. Truth table for standard SOP,POS expressions:

Inputs				Output
A	**B**	**C**	**D**	**F**
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Solved Examples: Digital Electronics

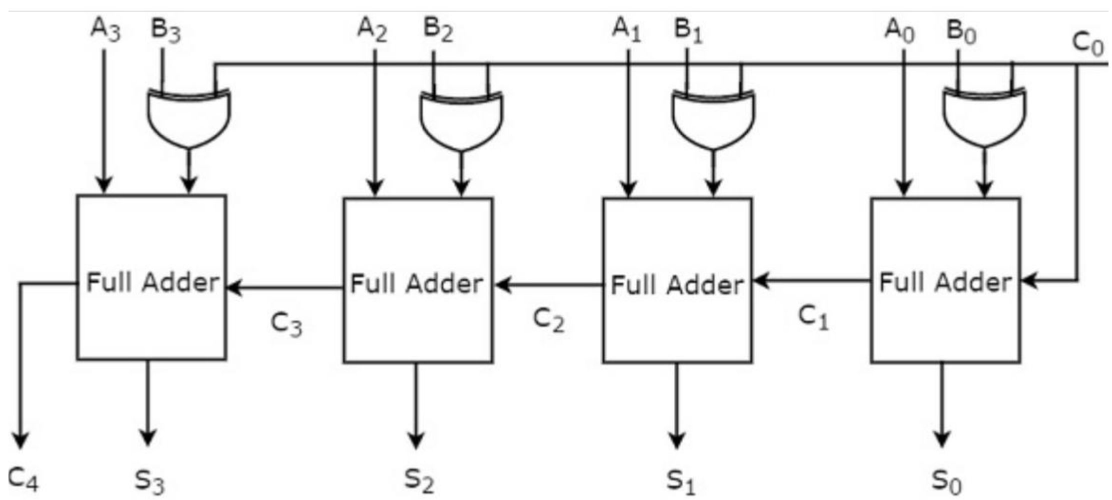
Ex. 12) *Design a full- subtractor logical circuit block diagram using half- subtractor?*

Sol.



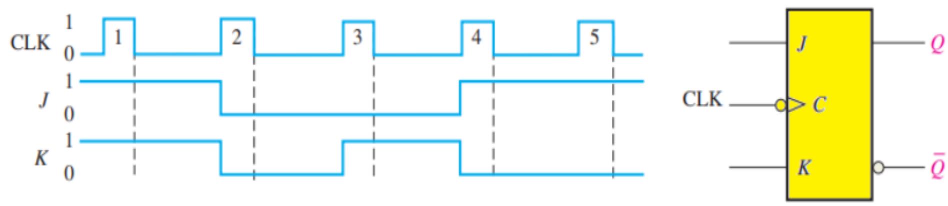
Ex. 13) *Design an adder/subtractor circuit using full-adders and gates?*

Sol.

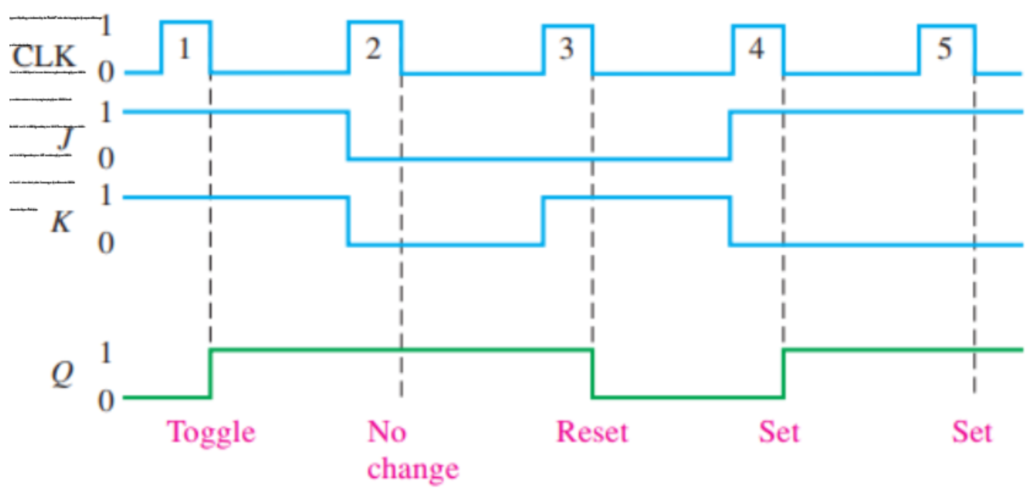


Solved Examples: Digital Electronics

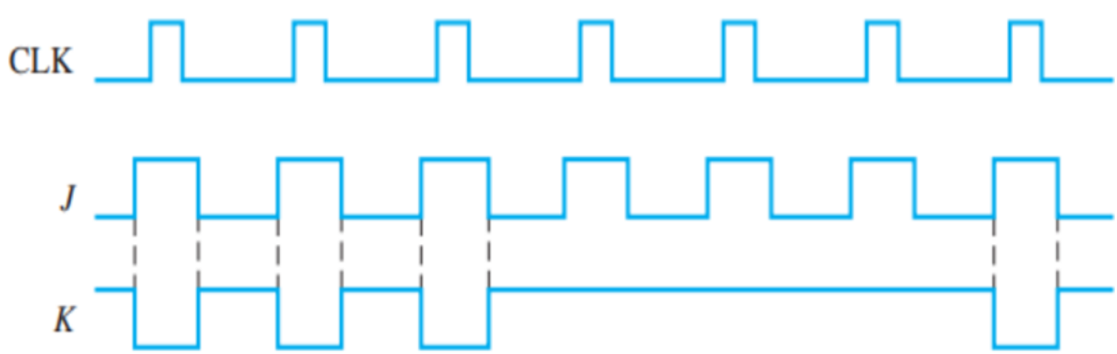
Ex.14) *The waveforms in figure below are applied to the **J, K** flip-flop and clock inputs as indicated. Determine the **Q** output, assuming that the flip-flop is initially RESET?*



Sol.

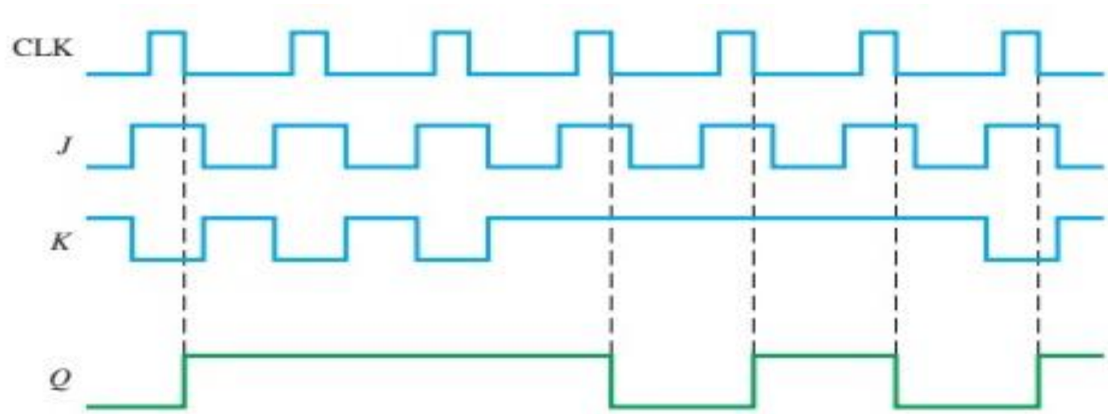


Ex.15) *For a negative edge-triggered **J-K** flip-flop with the inputs in figure below, develop the **Q** output waveform relative to the clock. Assume that Q is initially **LOW**?*

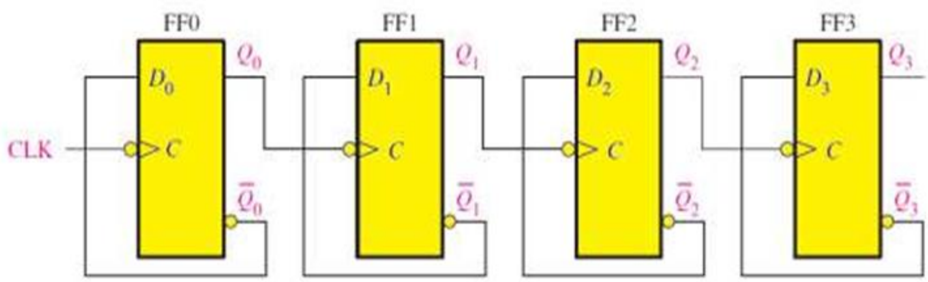


Solved Examples: Digital Electronics

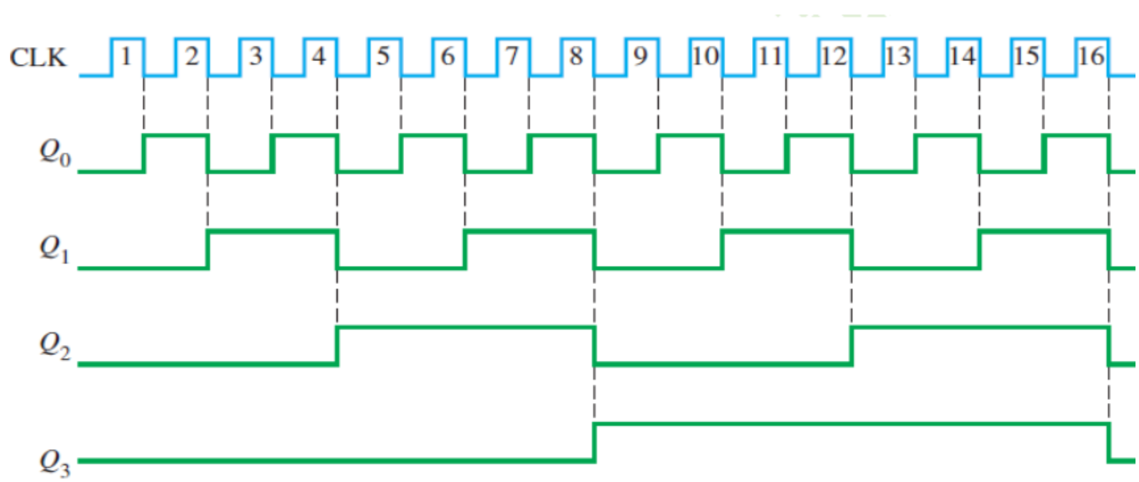
Sol.



Ex. 16) *Show the timing diagram if all of the flip-flops in the figure below are negative edge triggered. Begin with counter cleared?*



Sol.



Solved Examples: Digital Electronics

Ex. 17) *Put in canonical and standard SOP form from the following expression and draw the truth table, then determine canonical and standard POS form?*

$$F(A,B,C) = B + AC$$

Sol.

To find the missing variables we do:

A	B	C		A	B	C
0	1	0		0	0	1
0	1	1		0	1	1
1	1	0		1	0	1
1	1	1		1	1	1

Inputs			Output
A	*B*	*C*	*F*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Standard **SOP:**

$$F(A,B,C,D) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

Canonical **SOP:**

$$F(A,B,C,D) = \sum(1,2,3,\ 5,6,7)$$

Standard **POS:**

$$F(A,B,C) = (A + B + C)(\bar{A} + B + C)$$

Canonical **POS:**

$$F(A,B,C,D) = \prod(0,4)$$

Solved Examples: Digital Electronics

Ex. 18) *Using Boolean algebra techniques, simplify this expression:*

$$F = AB + A(B + C) + B(B + C)$$

Sol.

$$F = AB + AB + A\,C + B + BC$$

$$F = AB + A\,C + B + BC$$

$$F = A\,C + B(1 + A + C)$$

$$F = A\,C + B$$

Ex. 19) *Simplify the following Boolean expression*:

$$F = \overline{AB + AC} + \bar{A}\bar{B}C$$

Sol.

$$F = (\overline{AB})(\overline{AC}) + \bar{A}\bar{B}C$$

$$F = (\bar{A} + \bar{B})(\bar{A} + \bar{C}) + \bar{A}\bar{B}C$$

$$F = \bar{A} + \bar{A}\bar{C} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{B}C$$

$$F = \bar{A}(1 + \bar{C}) + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{B}C$$

$$F = \bar{A}(1 + \overline{B)} + \bar{B}\bar{C} + \bar{A}\bar{B}C$$

$$F = \bar{A}(1 + \bar{B}C) + \bar{B}\bar{C}$$

$$F = \bar{A} + \bar{B}\bar{C}$$

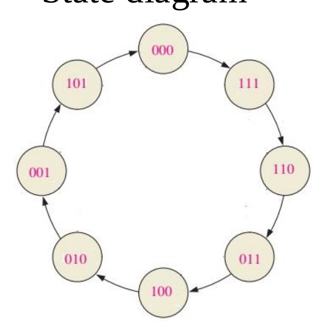
Ex. 20) *Design a synchronous counter that can count numbers* ***(0, 7, 6, 3, 4, 2, 1, and 5)*** *and repeat using* ***T Flip Flop****?*

Sol.

No. of state = N $=2^n = 2^3 = 8$

Max. of count = N-1 = 8-1 = 7

State diagram



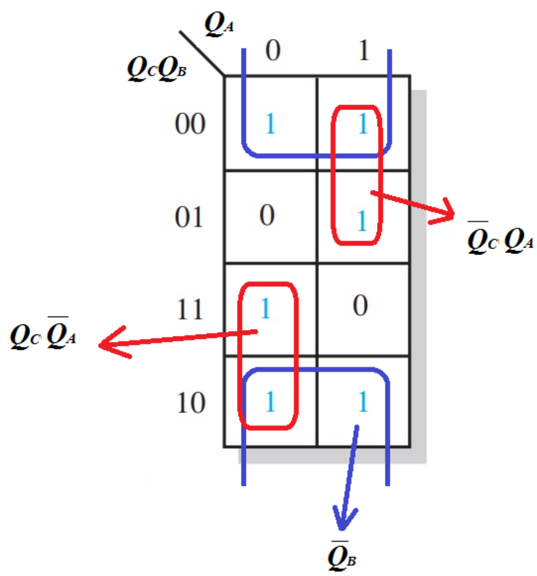
Solved Examples: Digital Electronics

Present state			Next state			Transition F.F. table		
Q_C	Q_B	Q_A	Q_C	Q_B	Q_A	T_C	T_B	T_A
0	0	0	1	1	1	1	1	1
1	1	1	1	1	0	0	0	1
1	1	0	0	1	1	1	0	1
0	1	1	1	0	0	1	1	1
1	0	0	0	1	0	1	1	0
0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	1	0	0
1	0	1	0	0	0	1	0	1

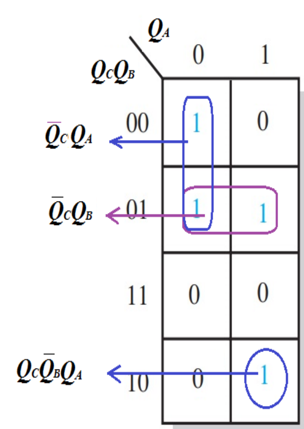
F.Fs. input expressions using K-map

$$T_C = \bar{Q}_C Q_A + Q_C \bar{Q}_A + \bar{Q}_B$$

$$T_C = (Q_C \oplus Q_A) + \bar{Q}_B$$

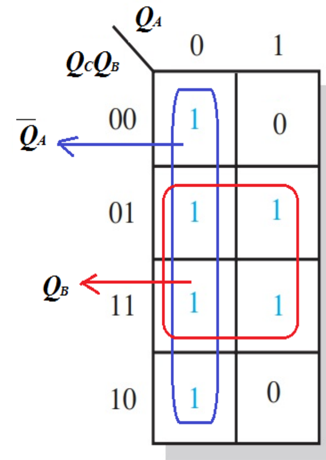


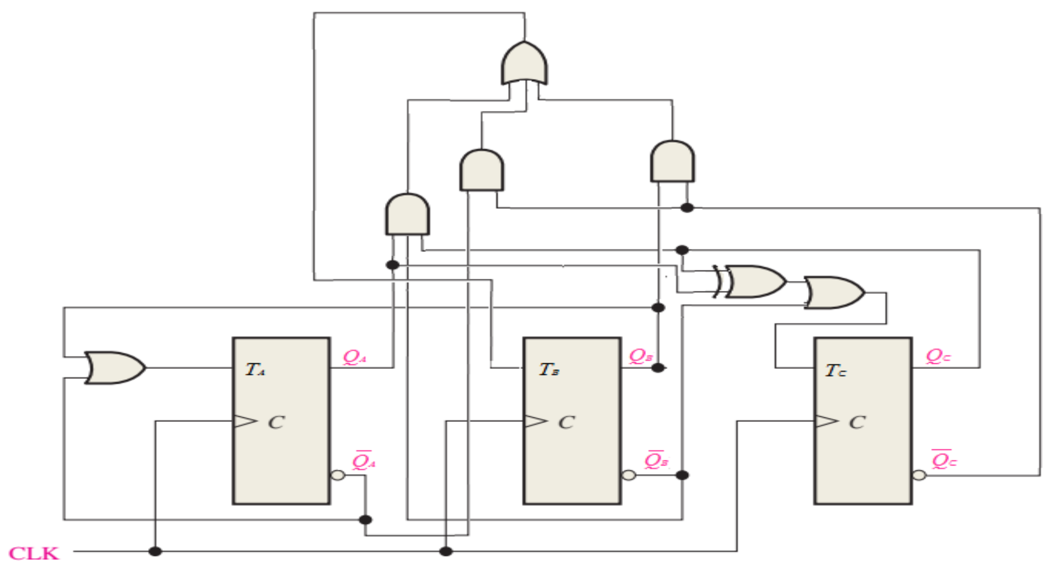
$$T_B = Q_C \bar{Q}_B Q_A + \bar{Q}_C \bar{Q}_A + \bar{Q}_c Q_B$$



Solved Examples: Digital Electronics

$$T_A = \overline{Q}_A + Q_B$$





Ex. 22) *Simplify the function using K-map:*

$$F = (\overline{A} + \overline{B} + \overline{C})(B + D)$$

Sol.

1. To substitute the values of the variables in K-map we must find the missing variables:

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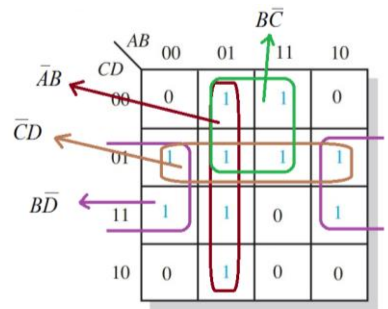
$\overline{A}$	$\overline{B}$	$\overline{C}$	D	A	B	C	D
1	1	1	0	0	0	0	0
1	1	1	1	0	0	1	0
				1	0	0	0
				1	0	1	0

2. The standard POS for F (A, B, C, D) is:

$$F(A,B,C,D) = (A+B+C+D)(A+B+\overline{C}+A)(\overline{A}+B+C+D)(\overline{A}+B+\overline{C}+D)(\overline{A}+\overline{B}+\overline{C}+D)\ (\overline{A}+\overline{B}+\overline{C}+\overline{D})$$



3. Minimal expression using K-map:

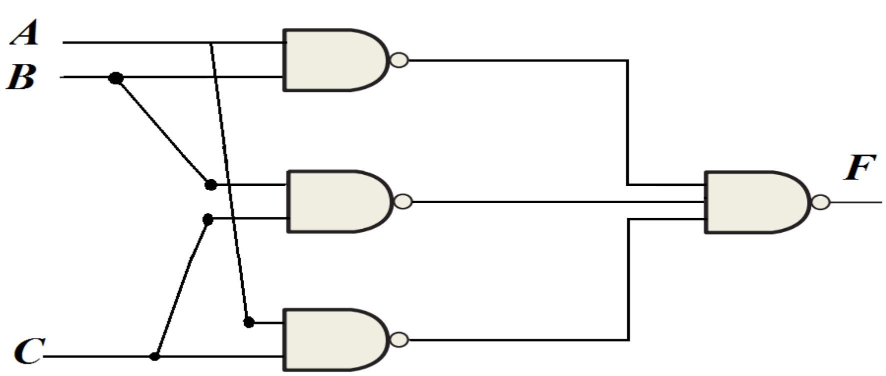
   Min. **SOP**:

$$F(A,B,C,D) = \overline{A}B + B\overline{C} + \overline{C}D + \overline{B}D$$

Ex. 23) *Using NAND gate to design a logic circuit has three input variables A, B, and C, and the output will be high only when a majority of the input high?*

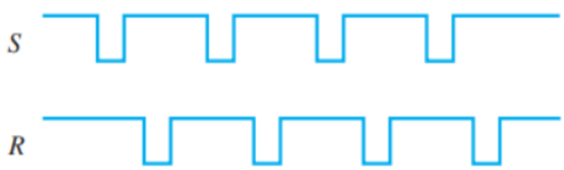
$$F(A,B,C) = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$
$$F(A,B,C) = \overline{A}BC + A\overline{B}C + AB(\overline{C} + C)$$
$$F(A,B,C) = \overline{A}BC + A(\overline{B}C + B)$$
$$F(A,B,C) = \overline{A}BC + AB + AC$$
$$F(A,B,C) = B(\overline{A}C + A) + AC$$
$$F(A,B,C) = B(C + A) + AC$$
$$F(A,B,C) = AB + BC + AC$$

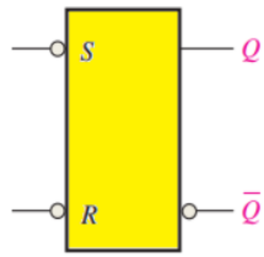
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



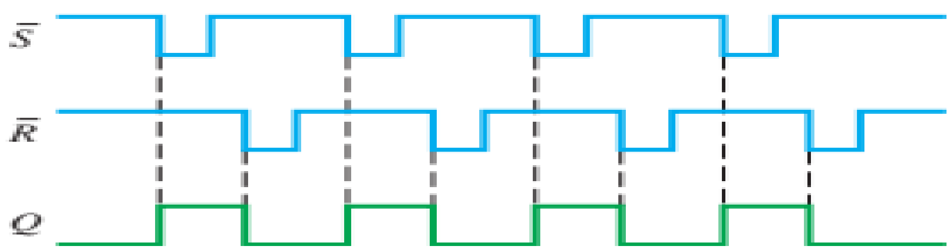
Solved Examples: Digital Electronics

Ex. 24) *If the waveforms in figure below are applied to an* ***active HIGH S-R latch****, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts LOW?*

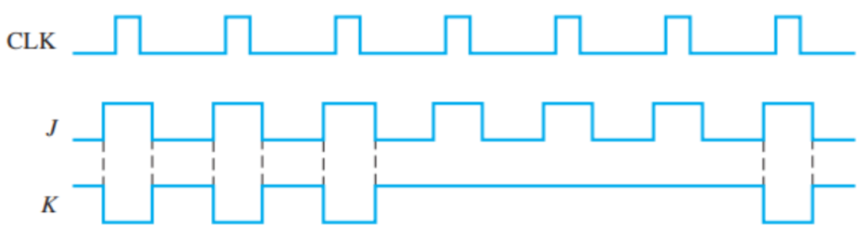




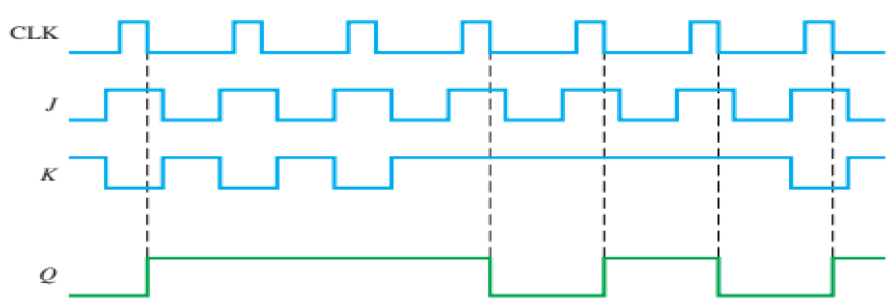
Sol.



Ex. 25) *For a* ***negative edge-triggered J-K*** *flip-flop with the inputs in figure below, develop the Q output waveform relative to the clock. Assume that* ***Q is initially LOW****?*

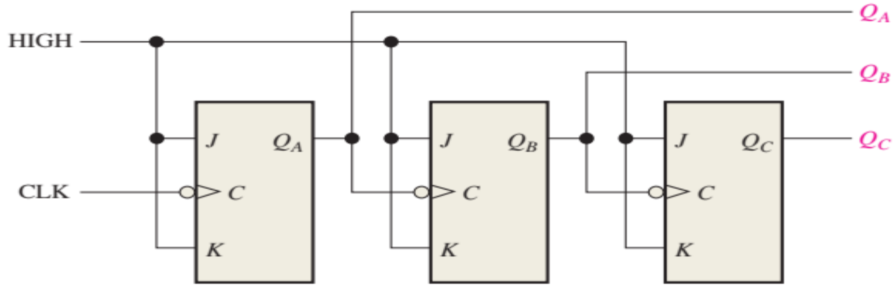


Sol.

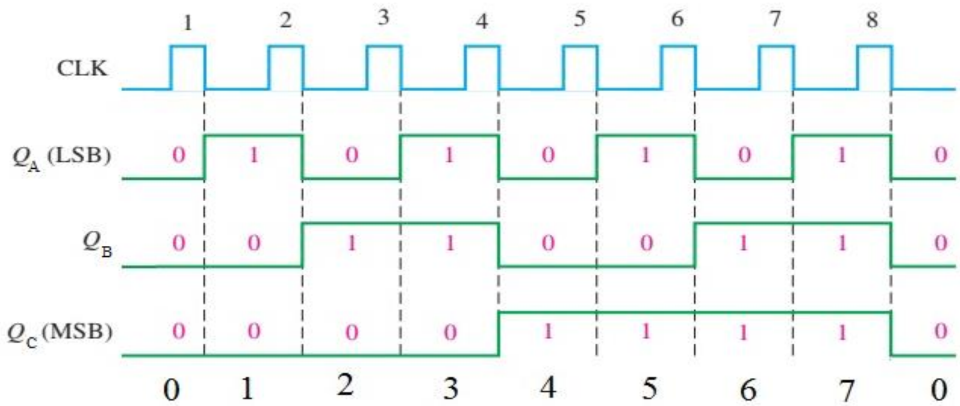


Solved Examples: Digital Electronics

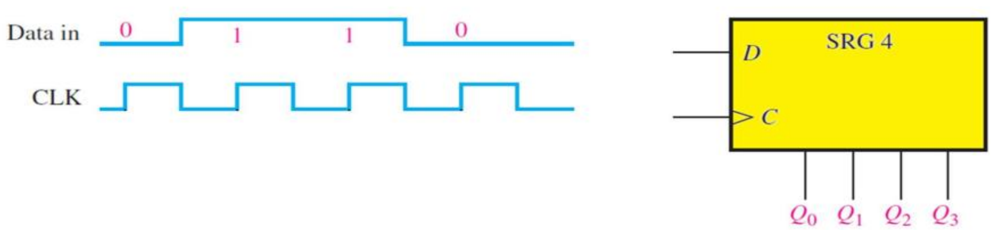
Ex. 26) Determine the output waveforms in relation to the clock for **Q_A, Q_B, and Q_C** in the circuit of Figure below and show the binary sequence represented by these waveforms. Begin with counter cleared?



Sol.



Ex. 27) ***4-bit** register **(SRG 4)** for the data input and clock waveforms in the figure below. The register initially contains all **1s**. If the data input remains **0** after the **fourth clock pulse**, what is the state of the register after **three additional clock pulses**?*



Sol.