COMMON-EMITTER CONFIGURATION

- The ***common-emitter configuration*** is the most frequently encountered transistor configuration appears in Fig. 5 for the *pnp* and *npn* transistors.
- Because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals).

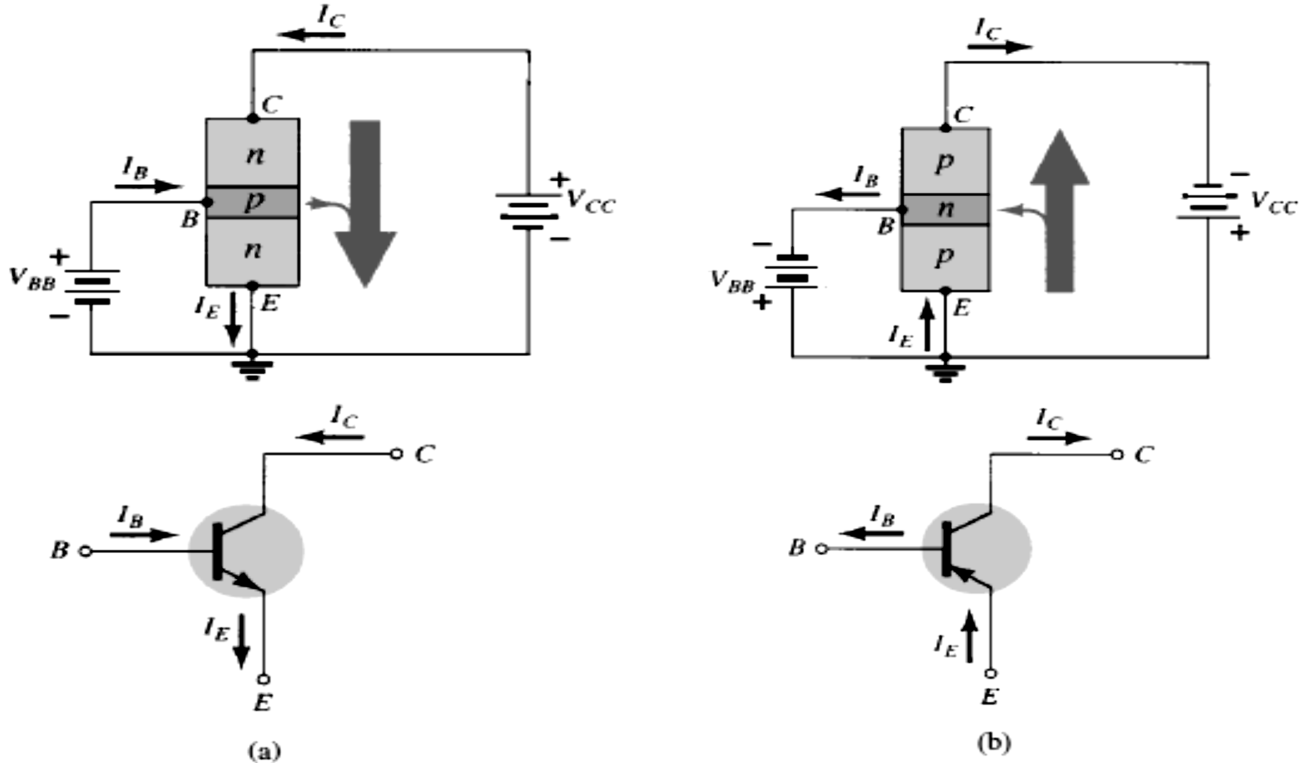


Figure (5) *Notation and symbols used with the common-emitter configuration:(a) npn transistor;(b) pnp transistor.*

- Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration:
- one for the *input* or *base–emitter* circuit and one for the *output* or *collector–emitter* circuit. Both are shown in Figure (6).

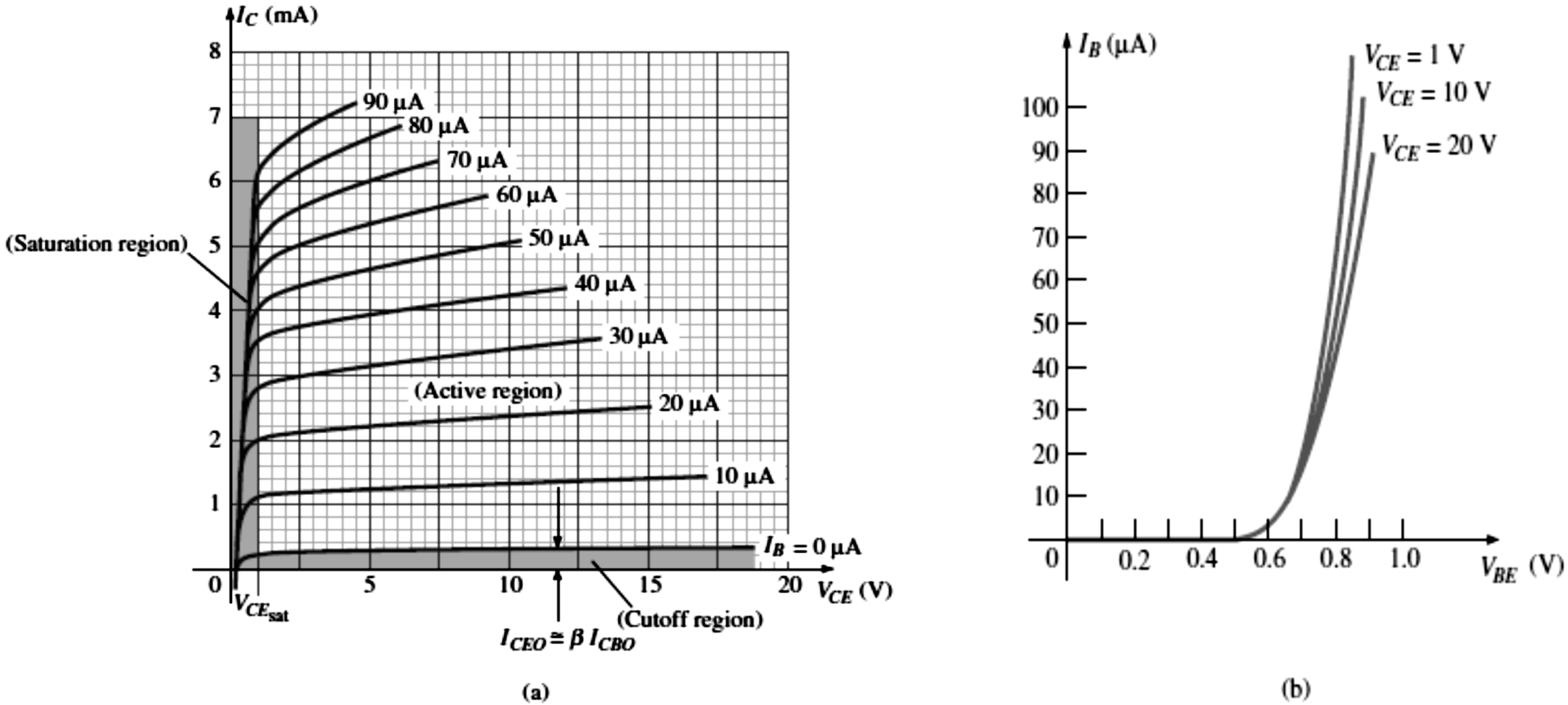


Figure (6) *Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.*

- For the common-emitter configuration, the current relations developed earlier for the common-base configuration are still applicable. That is, $I_E = I_C + I_B$ and $I_C = \alpha I_E$.
- Note that on the characteristics of Figure (6) that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to emitter voltage will influence the magnitude of the collector current.
- The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity.
- ***In the active region of a common-emitter amplifier, the base–emitter junction is forward-biased, whereas the collector–base junction is reverse-biased.***
- The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

- In Figure (6)a The region to the left of V_{CE} **sat** is called the saturation region.
- The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration.
- Note on the collector characteristics of Figure (6) that I_C is not equal to zero when I_B is zero.
- Substitution Eq. (1) in Eq. (4)
- $I_C = \alpha(I_C + I_B) + I_{CBO}$
- Rearranging yields $I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$ **(6)**
- The collector current defined by the condition I_B = 0 mA will be assigned the notation indicated by the following equation:
- $I_{CEO} = \frac{I_{CBO}}{1-\alpha}$ **(7)**
- ***For linear (least distortion) amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.***
- When employed as a switch in the logic circuitry of a computer, a transistor will have two points of operation of interest: one in the cutoff and one in the saturation region.

- **EXAMPLE 2:**

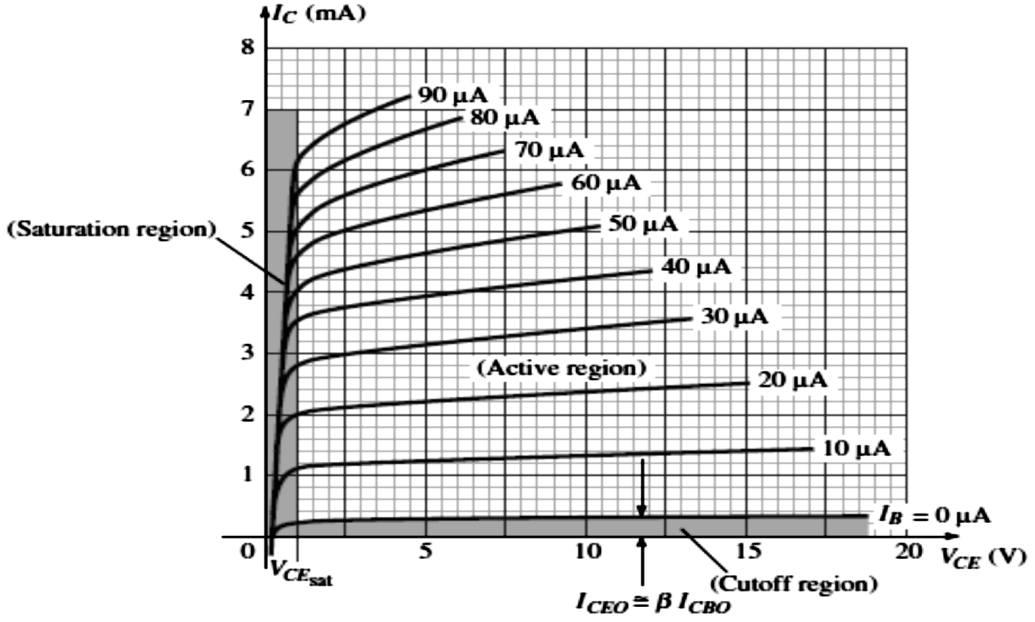
a. Using the characteristics of Figure (6), determine I_C at I_B = 30 mA and V_{CE} = 10 V.

b. Using the characteristics of Figure (6), determine I_C at V_{BE} = 0.7 V and V_{CE} = 15 V.

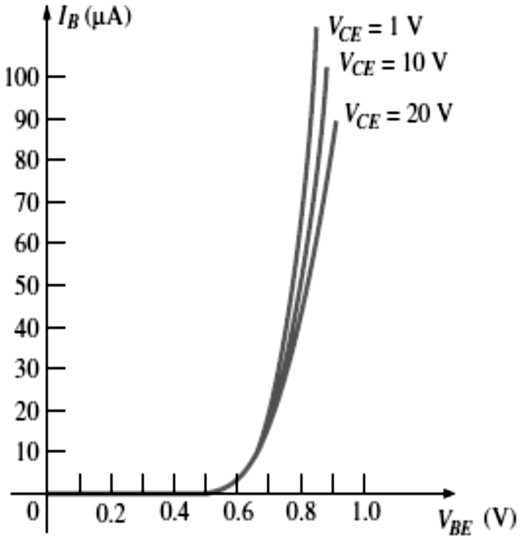
- ***Solution:***

a. At the intersection of I_B = 30 mA and V_{CE} = 10 V, I_C = **3.4 mA** .

b. Using Figure (6)b , we obtain I_B = 20 mA at the intersection of V_{BE} = 0.7 V and V_{CE} =15 V (between V_{CE} = 10 V and 20 V). From Figure (6)a we find that I_C = **2.5 mA** at the intersection of I_B = 20 mA and V_{CE} = 15 V.



(a)



(b)

- **Beta (B)**
- **DC Mode** In the dc mode the levels of I_C and I_B are related by a quantity called ***beta*** and defined by the following equation:
- $$\beta_{dc} = \frac{I_C}{I_B} \qquad \textbf{(8)}$$
- For practical devices the level of b typically ranges from about 50 to over 400, with most in the midrange.
- On specification sheets βdc is usually included as h_{FE} with the italic letter ***h*** derived from an **ac *h*ybrid** equivalent circuit to be introduced later.
- **AC Mode** For ac situations an ac beta is defined as follows:
- $$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=\text{constant}} \qquad \textbf{(9)}$$
- On specification sheets **βac** is normally referred to as h_{fe} . .

- A relationship can be developed between β and α using the basic relationships
- $$\alpha = \frac{\beta}{\beta+1} \quad (10)$$
- $$\beta = \frac{\alpha}{1-\alpha} \quad (11)$$
- $$I_{CEO} = (\beta + 1)I_{CBO}$$
- or
- $$I_{CEO} = \beta\, I_{CBO} \quad (12)$$
- $$I_C = \beta\, I_B \quad (13)$$
- we have
- $$I_E = (\beta + 1)I_B \quad (14)$$

- **Breakdown Region**
- As with the common-base configuration, there is a maximum collector-emitter voltage that can be applied and still remain in the active stable region of operation as shown in Figure (7).
- At high levels of base current, the currents almost climb vertically, whereas at lower levels a region develops that seems to back up on itself.
- This region is particularly noteworthy because an increase in current is resulting in a drop in voltage—totally different from that of any resistive element where an increase in current results in an increase in potential drop across the resistor, these regions are said to have a **negative-resistance** characteristic
- The recommended maximum value for a transistor under normal operating conditions is labeled BV_{CEO} as shown in Figure (7).
- BV_{CEO} less than BV_{CBO} and in fact, is often half the value of BV_{CBO}. Because of the **avalanche breakdown** mentioned before, and **punch-through**, is due to the **Early Effect**.
- In total the avalanche effect is dominant because any increase in base current due to the breakdown phenomena will be increase the resulting collector current by a factor beta.

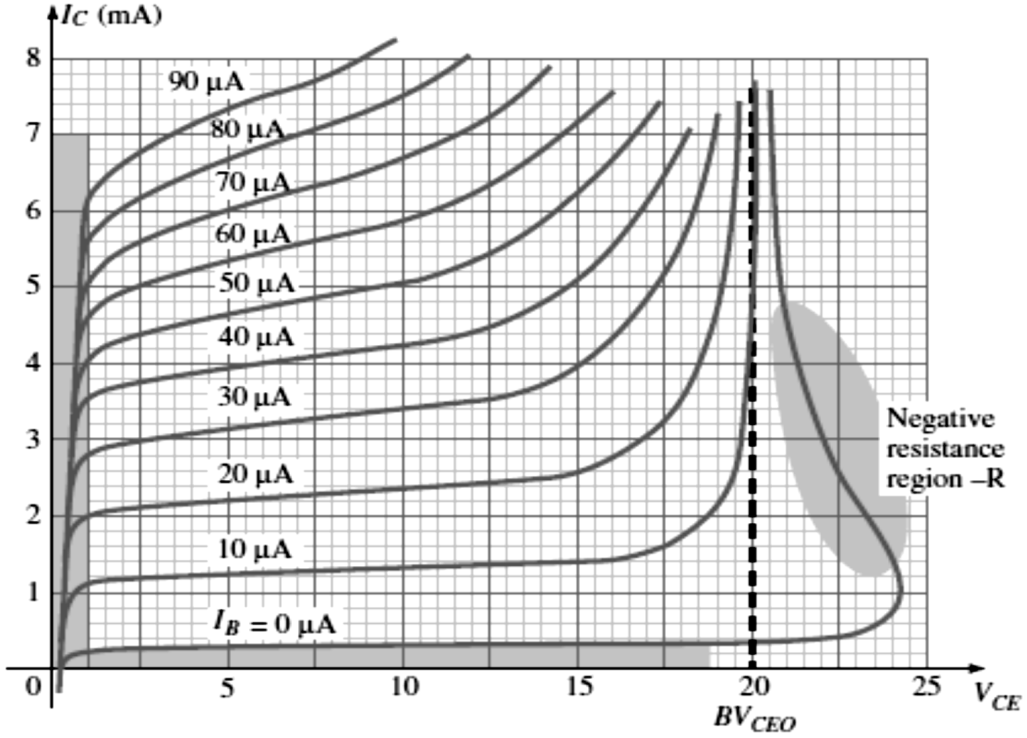


Figure (7) *Examining the breakdown region of a transistor in the common-emitter configuration.*

COMMON-COLLECTOR CONFIGURATION

- The final transistor configuration is the *common-collector configuration,* shown in Figure (8) with the proper current directions and voltage notation.
- The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common emitter configurations.

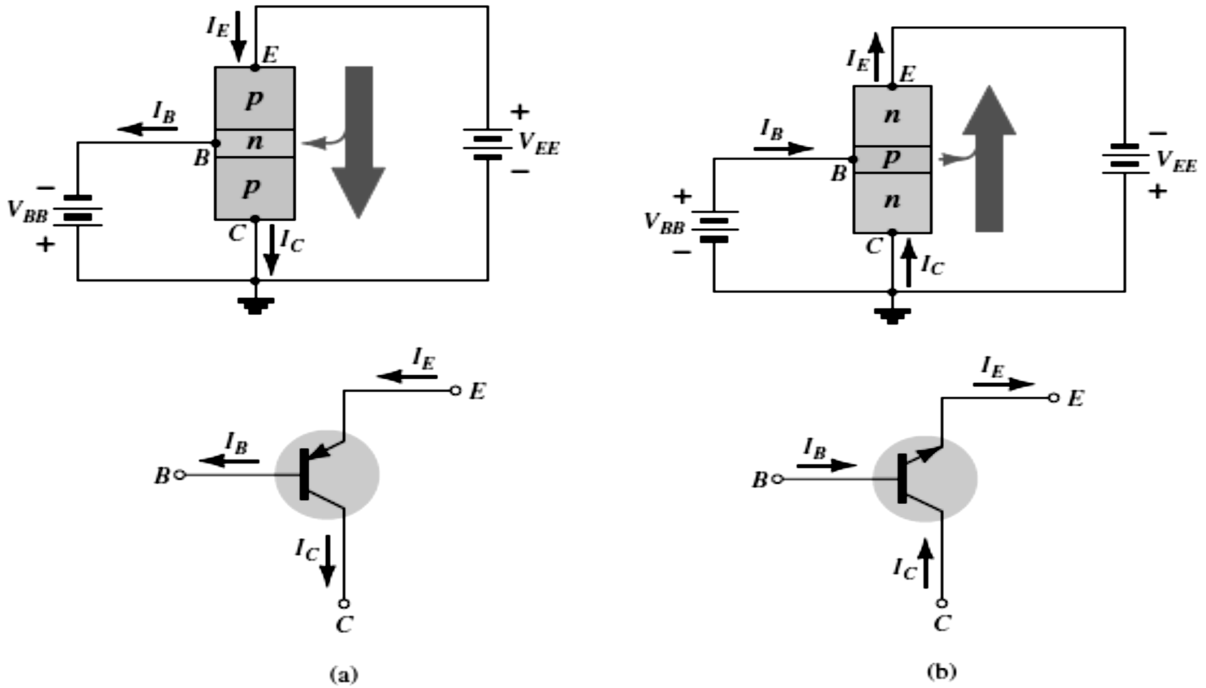


Figure (8) *Notation and symbols used with the common-collector configuration: (a) pnp transistor;(b) npn transistor.*

- A common-collector circuit configuration is provided in Figure (9) with the load resistor connected from emitter to ground.
- The output characteristics of the common-collector configuration is the same as for the common-emitter configuration.
- For the common-collector configuration the output characteristics are a plot of I_E versus V_{CE} for a range of values of I_B.
- The input current, therefore, is the same for both the common emitter and common-collector characteristics.
- The horizontal voltage axis for the common collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics.

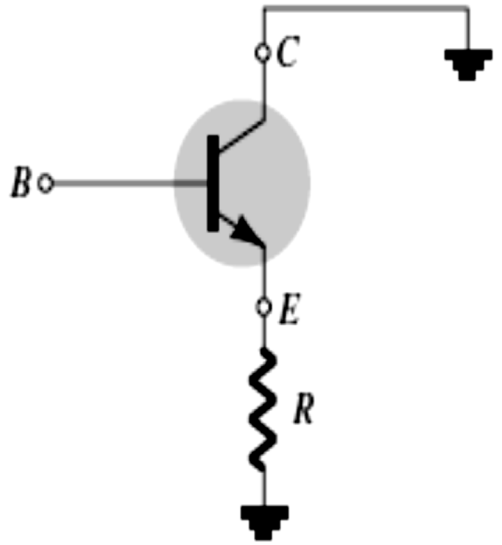


Figure (9) *Common-collector configuration used for impedance-matching purposes.*

LIMITS OF OPERATION

- For each transistor there is a region of operation on the characteristics that will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion.
- As example for the transistor of Figure (10), $\boldsymbol{I_{C\max}}$ was specified as 50 mA and $\boldsymbol{BV_{CEO}}$ as 20 V. The vertical line on the characteristics defined as $\boldsymbol{V_{CE\text{sat}}}$ specifies the minimum $\boldsymbol{V_{CE}}$ that can be applied without falling into the nonlinear region labeled the *saturation* region.
- The level of $\boldsymbol{V_{CE\text{sat}}}$ is typically in the neighborhood of the 0.3 V specified for this transistor.
- The maximum dissipation level is defined by the following equation:
- $$P_{C\max} = V_{CE}I_C \qquad \textbf{(15)}$$

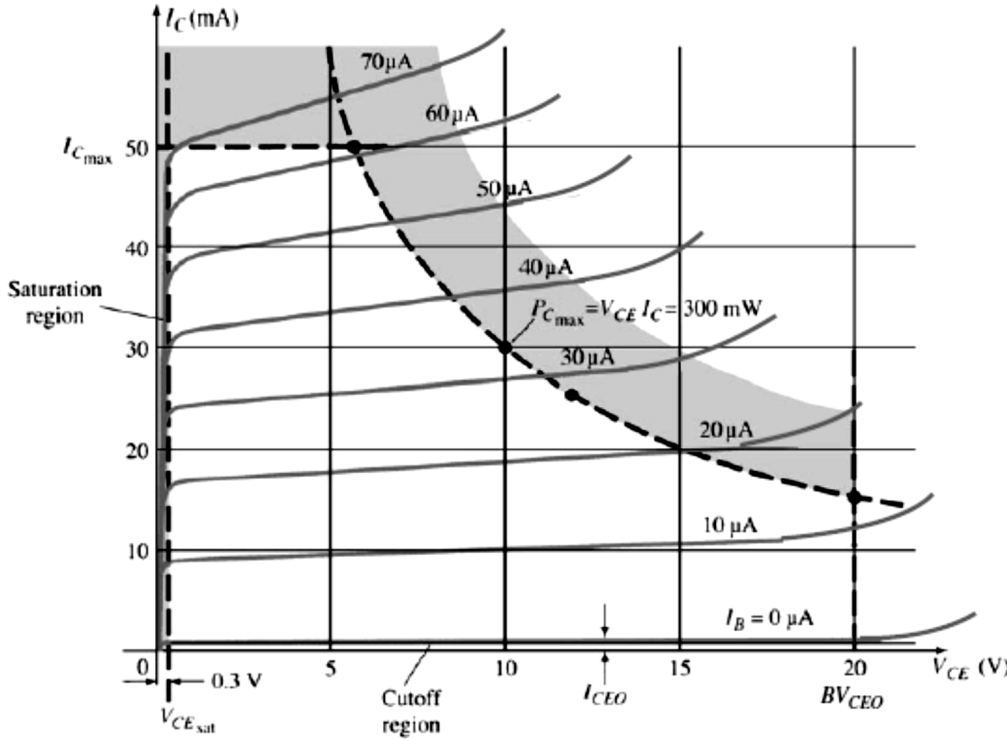


Figure (10) *Defining the linear (undistorted) region of operation for a transistor.*

- If the characteristic curves are unavailable or do not appear on the specification sheet (as is often the case), one must simply be sure that I_C, V_{CE}, and their product $V_{CE} I_C$ fall into the following range:
- $$I_{CEO} \leq I_C \leq I_{Cmax}$$
- $$V_{CEsat} \leq V_{CE} \leq V_{CEmax} \qquad (16)$$
- $$V_{CE}I_C \leq P_{Cmax}$$
- For the common-base characteristics the maximum power curve is defined by the following product of output quantities:
- $$P_{Cmax} = V_{CB}I_C \qquad (17)$$