UNIVERSITY OF BABYLON
COLLEGE OF SCIENCE FOR WOMEN
COMPUTER DEPARTMENT

2024 / 2025
FIRST CLASS

Computer Skills

LECTURES

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❖ LEARNING OBJECTIVES

After completion of this lecture, you should be able to:

- Describe the main memory unit.
- Describe the *Memory chips*
- Describe the basic memory operations

1. MAIN MEMORY UNIT

A computer cannot work without some form of memory. Because disk drives are extremely slow compared with the speed of the CPU, using them as the main processor memory make the whole system very slow. The processor will spend more of its time waiting to access the disk drive than carrying out program instructions. For this reason, the main memory where application and other support programs are loaded must have a speed comparable with that of the CPU itself. This means a memory store in the form of integrated circuits or chips. ***The main memory provides the main storage for a computer***.

Figure 1 shows a typical interface between the main memory and the CPU. Two CPU registers are used to interface the CPU to the main memory. These are the ***memory address register* (MAR)** and the ***memory data register* (MDR)**. The MDR is used to hold the data to be stored and/or retrieved in/from the memory location whose address is held in the MAR.

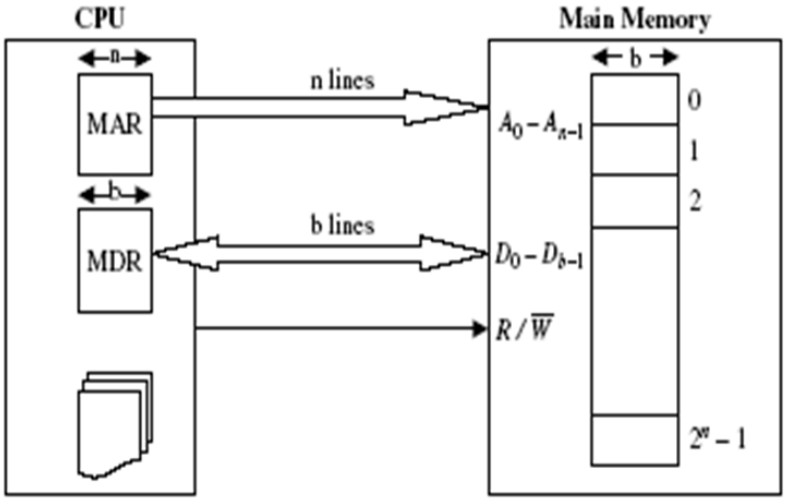


FIGURE 1.A TYPICAL CPU AND MAIN MEMORY INTERFACE

The memory of a computer system consists of tiny electronic switches, with each switch in one of two states: ***open*** or ***closed***. It is, however, more convenient to think of these states as **0** and **1**, rather than open and closed. Thus, each switch can represent a bit. The memory unit consists of millions of such bits. In order to make memory more manageable, eight bits are grouped into a byte. Memory can then be viewed as consisting of an ordered sequence of bytes. Each byte in this memory is identified by its sequence number starting with 0, as shown in Figure 2. This is referred to as the ***memory address*** of the byte. Such memory is called ***byte addressable*** memory because each byte has a unique address.

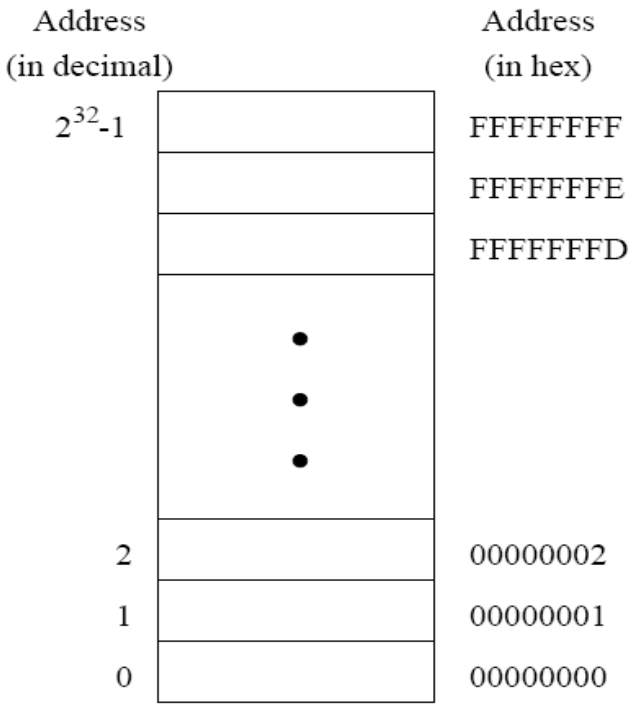


FIGURE 2.LOGICAL VIEW OF THE SYSTEM MEMORY.

The Pentium can address up to 4 GB (2^{32} bytes) of main memory (see Figure 2). This magic number comes from the fact that the address bus of the Pentium has 32 address lines. This number is referred to as the *memory address space*. The memory address space of a system is determined by the address bus width of the processor used in the system. The actual memory in a system, however, is always less than or equal to the memory address space. The amount of memory in a system is determined by how much of this memory address space is *populated* with memory chips.

1.1. MEMORY CHIPS

It is possible to visualize a typical internal main memory structure as consisting of rows and columns of basic cells. Each cell is capable of storing one bit of information. Figure 3 provides a conceptual internal organization of a memory chip. In this Figure, cells belonging to a given row can be assumed to form the bits of a given memory word. Address lines $\mathbf{A_0A_1 \ldots A_{n-2}A_{n-1}}$ are used as inputs to the address decoder in order to generate the word select lines $\mathbf{W_0\ W1 \ldots W_{2^n-1}}$. A given word select line is common to all memory cells in the same row. At any given time, the address decoder activates only one word select line while deactivating the remaining lines. A word select line is used to enable all cells in a row for read or write. Data (bit) lines are used to input or output the contents of cells. Each memory cell is connected to two data lines. A given data line is common to all cells in a given column.

The address lines $A_0 \ldots A_{n-1}$ in the memory chip shown in Figure 3 contain an address, which is decoded from an ***n*-bit** address into one of $\mathbf{2^n}$ **locations (***The number of locations may be obtained from the address width of the chip***)** within the chip, each of which has a ***w*-bit** word associated with it. The storage capacity of a memory chip is the product of the number of locations and the word width. The chip thus contains $\mathbf{2^n \times w}$ bits.

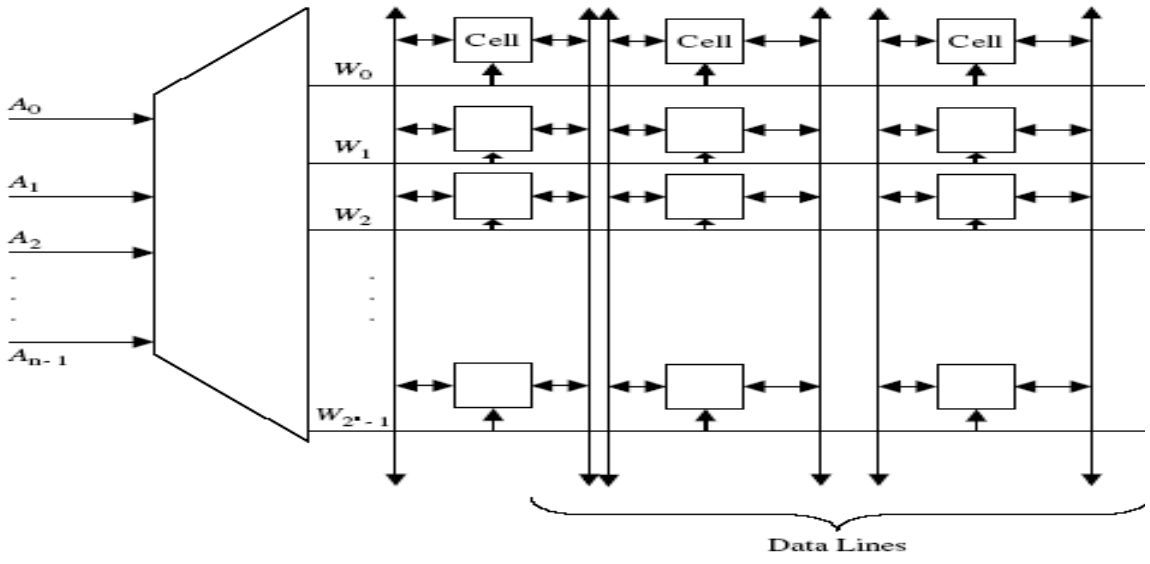


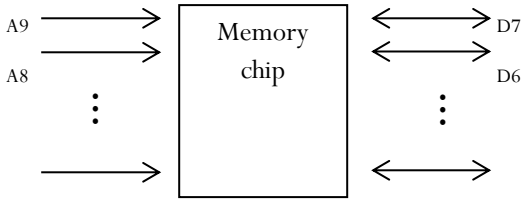
FIGURE 3.A CONCEPTUAL INTERNAL ORGANIZATION OF A MEMORY CHIP

The computer's word size can be the size of the data bus which carries data between the CPU and memory and the CPU and I/O devices.

To access the memory, to store or retrieve a single word of information, it is necessary to have a unique address. The word address is the number that identifies the location of a word in a memory.

For example, a chip width 10 address lines has 2^10=1024 locations. Given an 8 bit data width, a 10-bit address chip has a memory size of :

2^10 * 8 = 1024 * 8 = 1K * 1byte = Kbyte



10-bit address 8-bit data

The second properties of memory chips is access time, access time is the speed with a location within the memory chip may be made available to the data bus. It is defined as the time interval between the instant لحظةthat an address is sent to the memory chip and the instant that the data stored in the locations appears on the data bus. Access time is given in nanosecond's (ns) and varies from 25 ns to the relatively slow 200 ns.

In general a computer with a larger word size can execute programs of instructions at a faster rate because more data and more instructions are stuffed into word. The larger word sizes, however, mean more lines making up the data bus, and therefore more interconnections between the CPU and memory and I/O devices.

A single chip is usually insufficient to provide the memory requirements of a computer. A number of chips are therefore connected in parallel to form what is known as a ***memory bank***. Figure 4 below shows a memory bank consisting of eight 1Kbit chips. Each has 18 address lines (A_0 … A_{17}). The total storage capacity of one chip = **2^18 * 1** = **256 K bits**. Total size of the memory bank = **256 K bits × 8=256 KB**

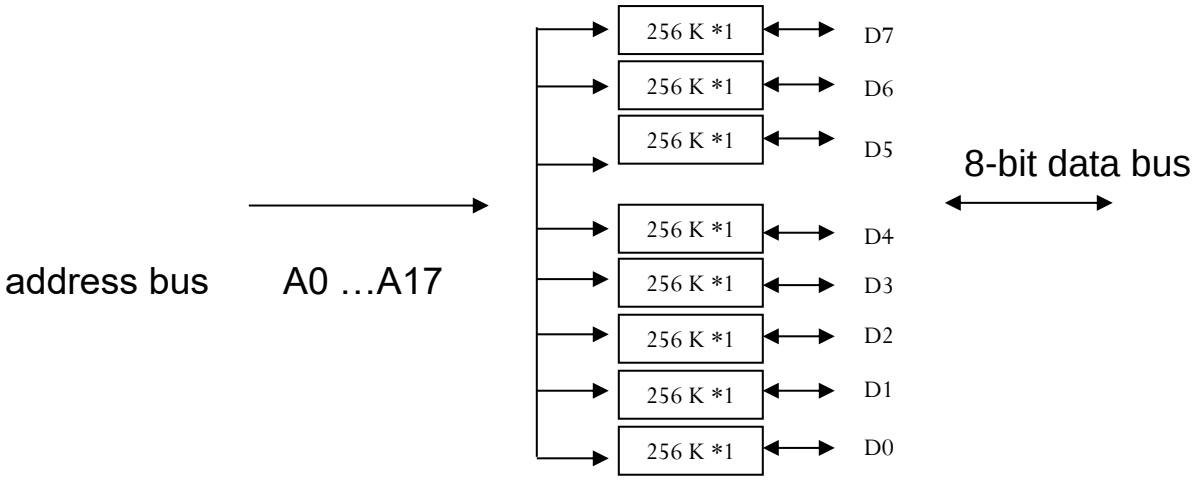


FIGURE 4.MEMORY BANK

Ex: A certain memory chip is specified as 2K×8

1- **How many words can be stored on this chip?**
2- **What is the word size :**
3- **How many total bits can this chip store?**

Solution:

1- 2K=2*1024=2048 words
2- The word size is 8-bits(1-byte)
3- Capacity = 2048 * 8=16384bits=16Kbit

2. BASIC MEMORY OPERATIONS

The memory unit supports two basic operations: read and write. The read operation reads previously stored data and the write operation stores a new value in memory. Both of these operations require a memory address. In addition, the write operation requires specification of the data to be written. The address and data of the memory unit are connected to the address and data buses of the system bus, respectively. The read and write signals come from the control bus. Two metricsمقياسين are used to characterize memory. Access time refers to the amount of time required by the memory to retrieve

the data at the addressed location. The other metric is the memory cycle time, which refers to the minimum time between successive المتعاقبة memory operations.

The read operation is nondestructive غير مدمرةin the sense that one can read a location of the memory as many times as one wishes without destroying the contents of that location. The write operation, however, is destructive, as writing a value into a location destroys the old contents of that memory location.

2.1. STEPS IN A TYPICAL READ CYCLE

1. Place the address of the location to be read on the address bus,
2. Activate the memory read control signal on the control bus,
3. Wait for the memory to retrieve the data from the addressed memory location and place them on the data bus,
4. Read the data from the data bus,
5. Drop the memory read control signal to terminate the read cycle.

2.2. STEPS IN A TYPICAL WRITE CYCLE

1. Place the address of the location to be written on the address bus,
2. Place the data to be written on the data bus,
3. Activate the memory write control signal on the control bus,
4. Wait for the memory to store the data at the addressed location,
5. Drop the memory write signal to terminate the write cycle.